FIG 1

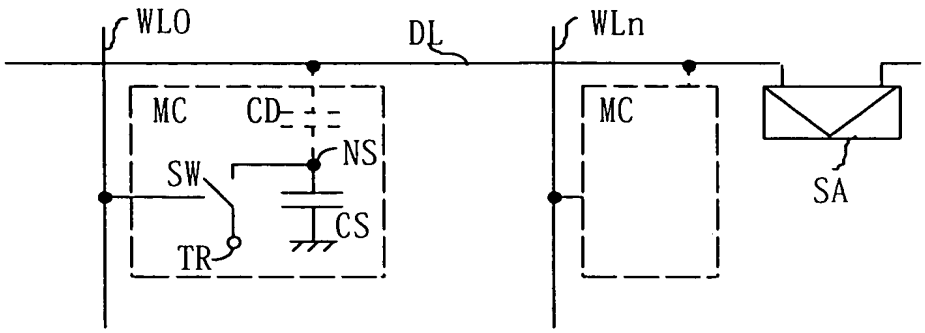


FIG 2A

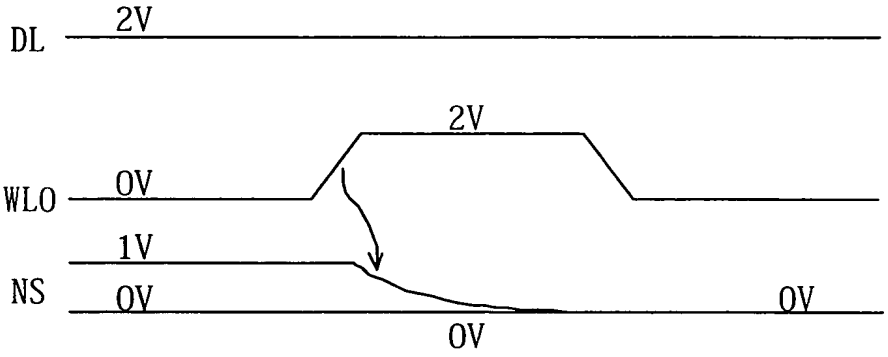


FIG 2B

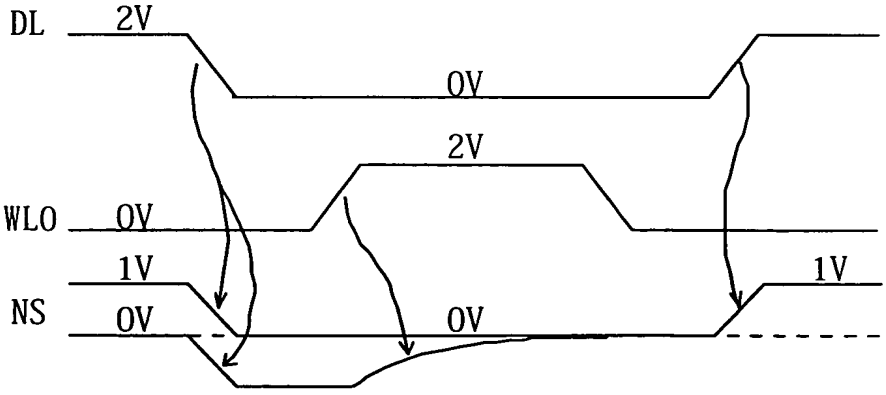


FIG 3

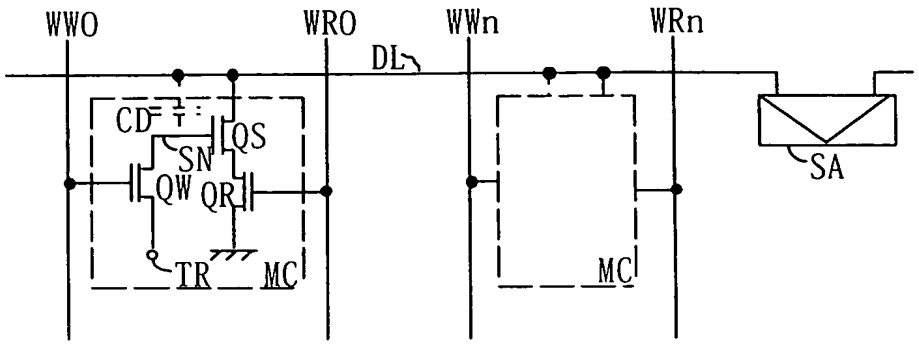


FIG 4A

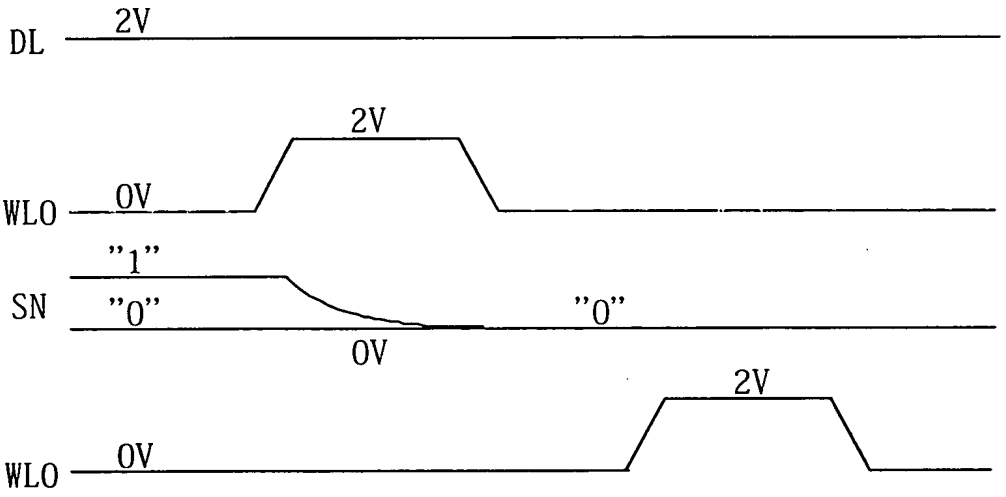


FIG 4B

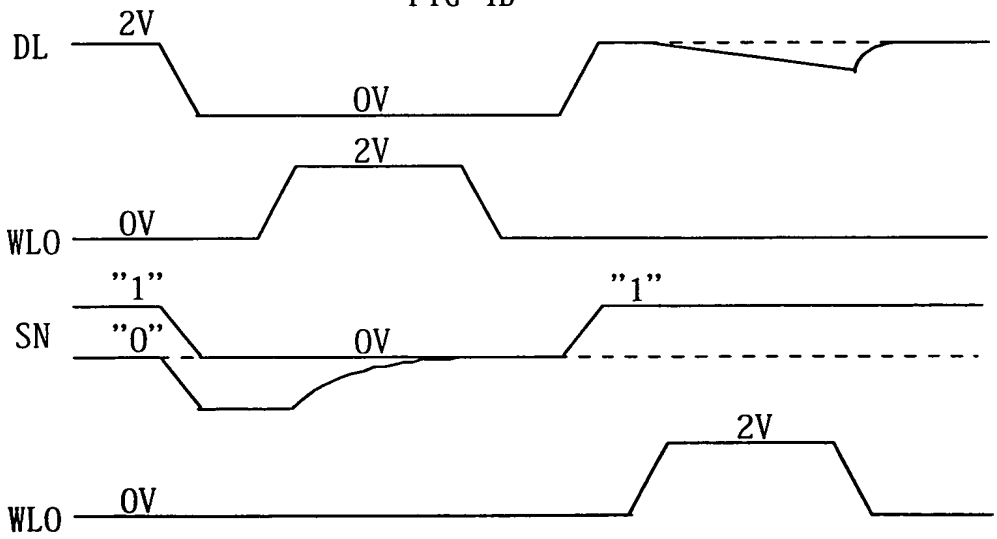


FIG 5
(Prior Art)

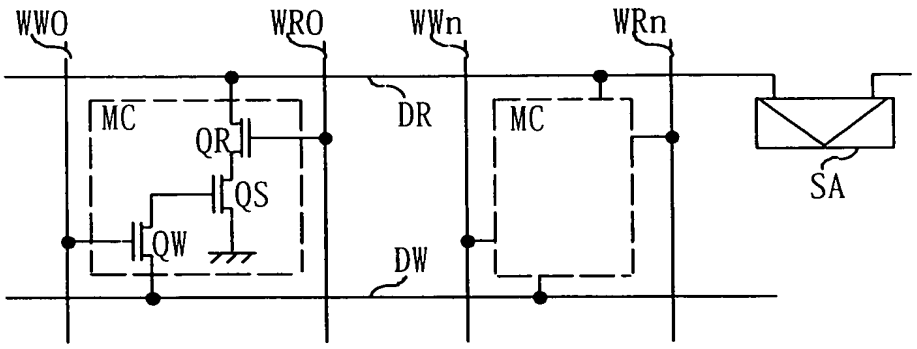


FIG 6A

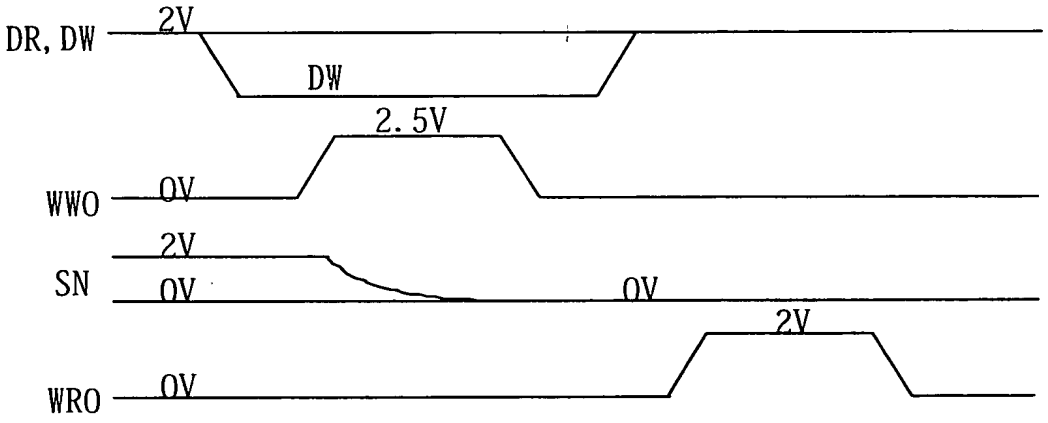


FIG 6B

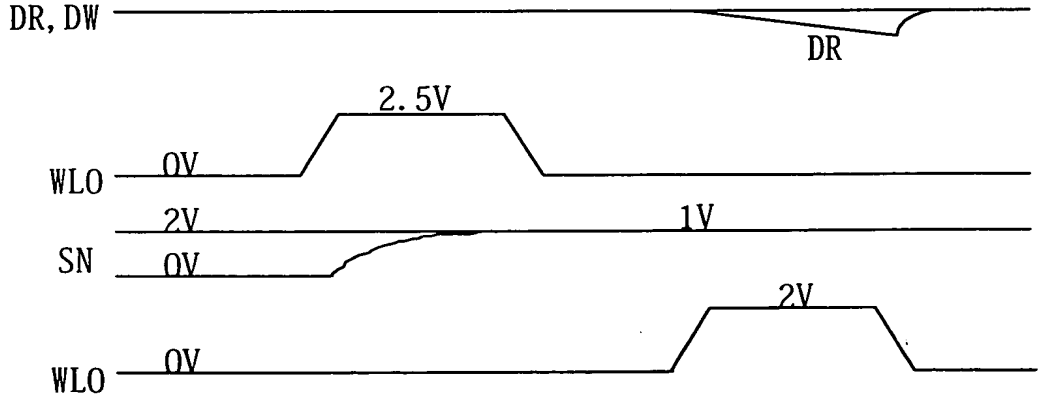
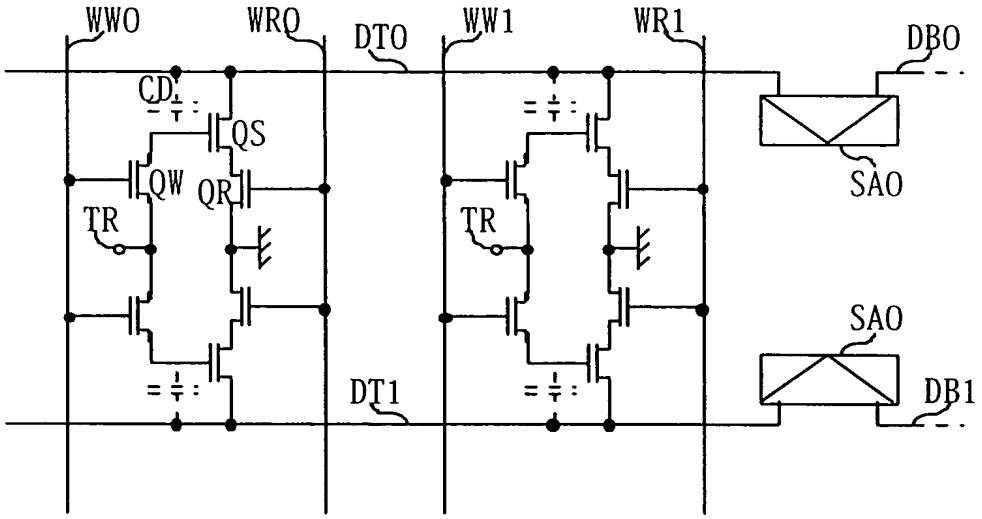


FIG 7



		WRITE			READ	STANDBY
		DATA SET	NODE CHARGE TRANSFER	NODE SHUTOFF		
	DTO, 1 "0" STATE	2V	2V	2V	FLOAT HIGH	2V
	DTO, 1 "1" STATE	0	0	0	FLOAT HIGH	2V
	WWO	0	2	0	0	0
	WRO	0	0	0	2V	0
	TR	0	0	0	0	0
	WW1, WR1	0	0	0	0	0

FIG 8

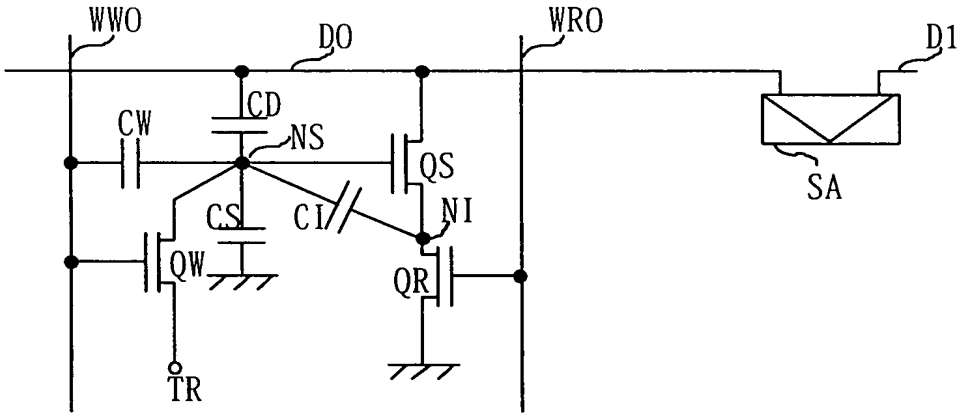

WWO
DO
WRO
D1
CD
CW
NS
QS
SA
CS
CI
NI
QW
QR
TR

FIG 9

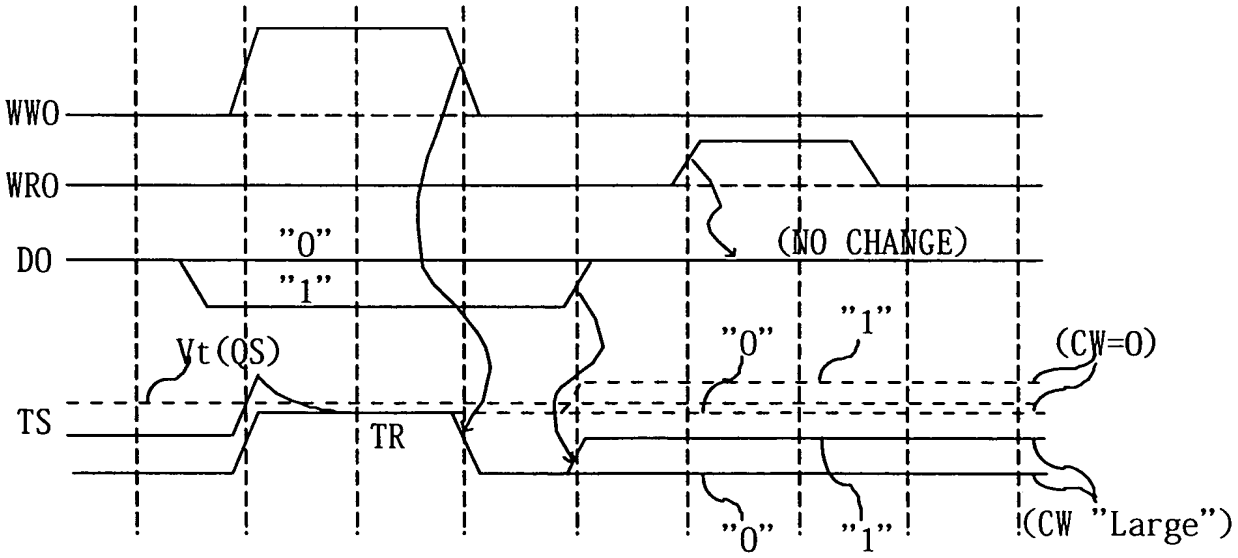

WWO
WRO
DO
"0"
"1"
(NO CHANGE)
Vt(QS)
TS
TR
"0"
"1"
(CW=0)
"0"
"1"
(CW "Large")

FIG 10

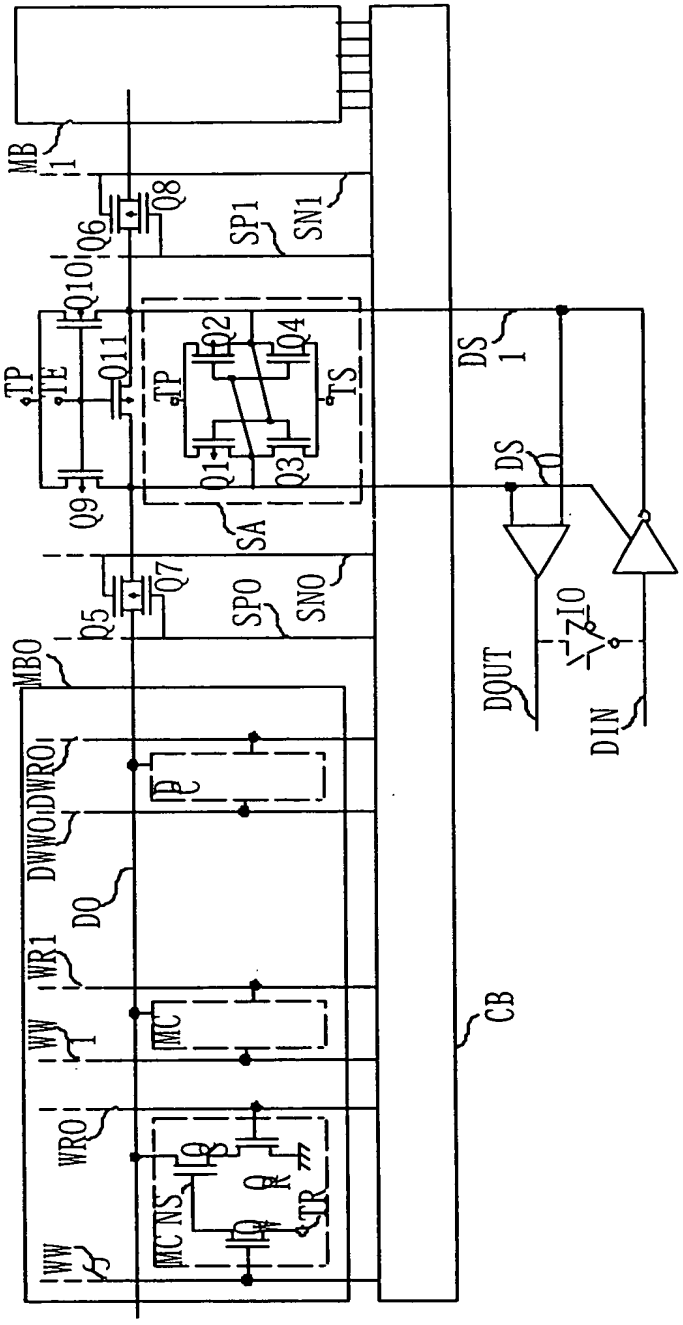

MB
1
Q8
Q6
SP1
SN1
Q10
Q11
Q2
Q4
TP
TE
TP
TS
DS
1
DS
0
Q1
Q3
Q9
SA
Q7
Q5
SPO
SNO
MBO
DOUT
IO
DIN
DWRO
DWWO
DQ
WR1
WW
1
MC
WRO
MCNS
Q
R
TR
WW
CB

FIG 11

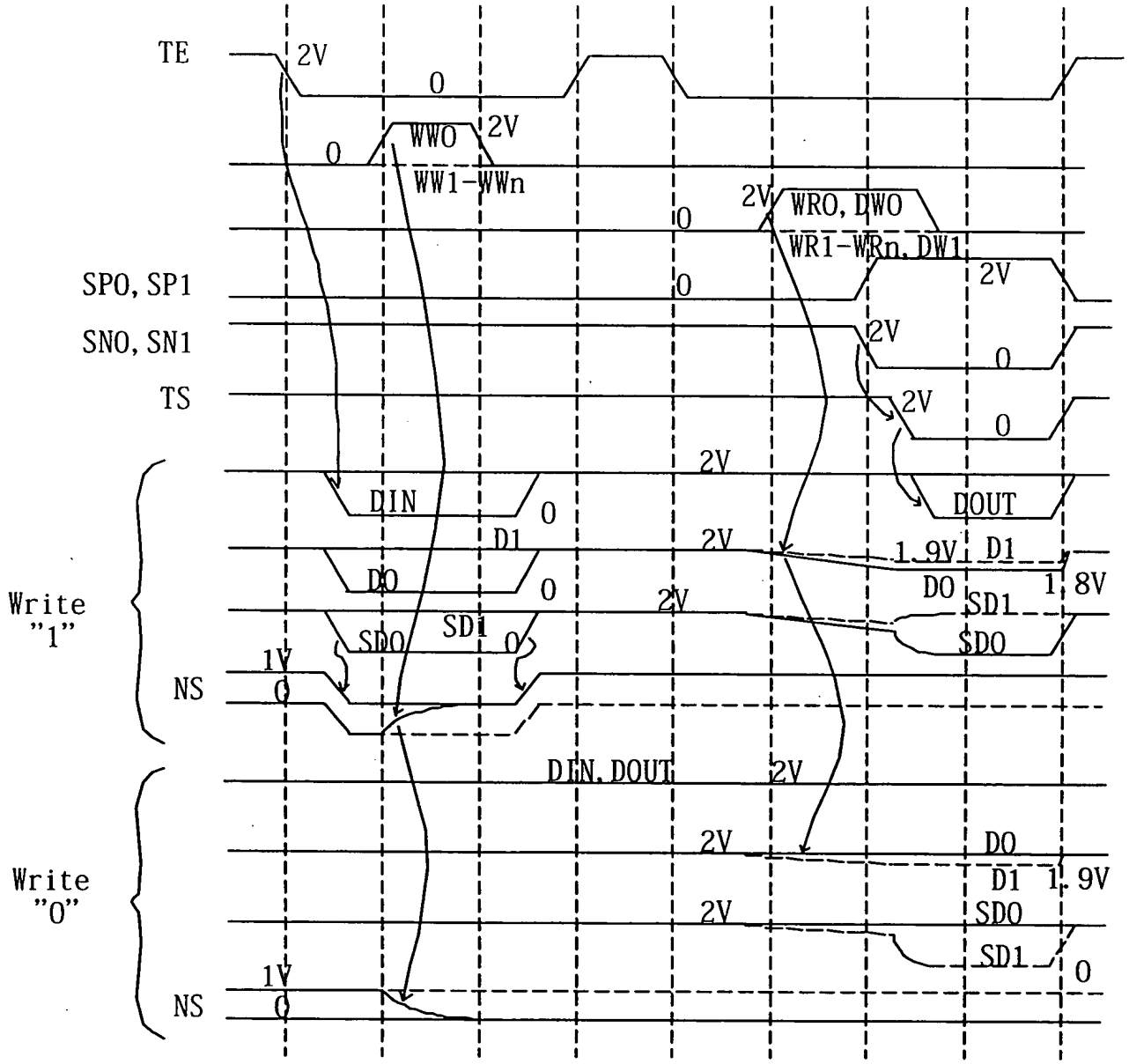

TE
2V
0
WWO
2V
0
WW1-WWn
2V
WRO, DWO
0
WR1-WRn, DW1
2V
SPO, SP1
0
SNO, SN1
2V
0
TS
2V
0
2V
DIN
0
DOUT
D1
2V
1.9V
D1
DO
0
DO
1.8V
2V
SD1
SD1
SDO
0
SDO
Write "1"
1V
NS
0
DIN, DOUT
2V
2V
DO
D1
1.9V
Write "0"
2V
SDO
SD1
0
1V
NS
0

FIG 12

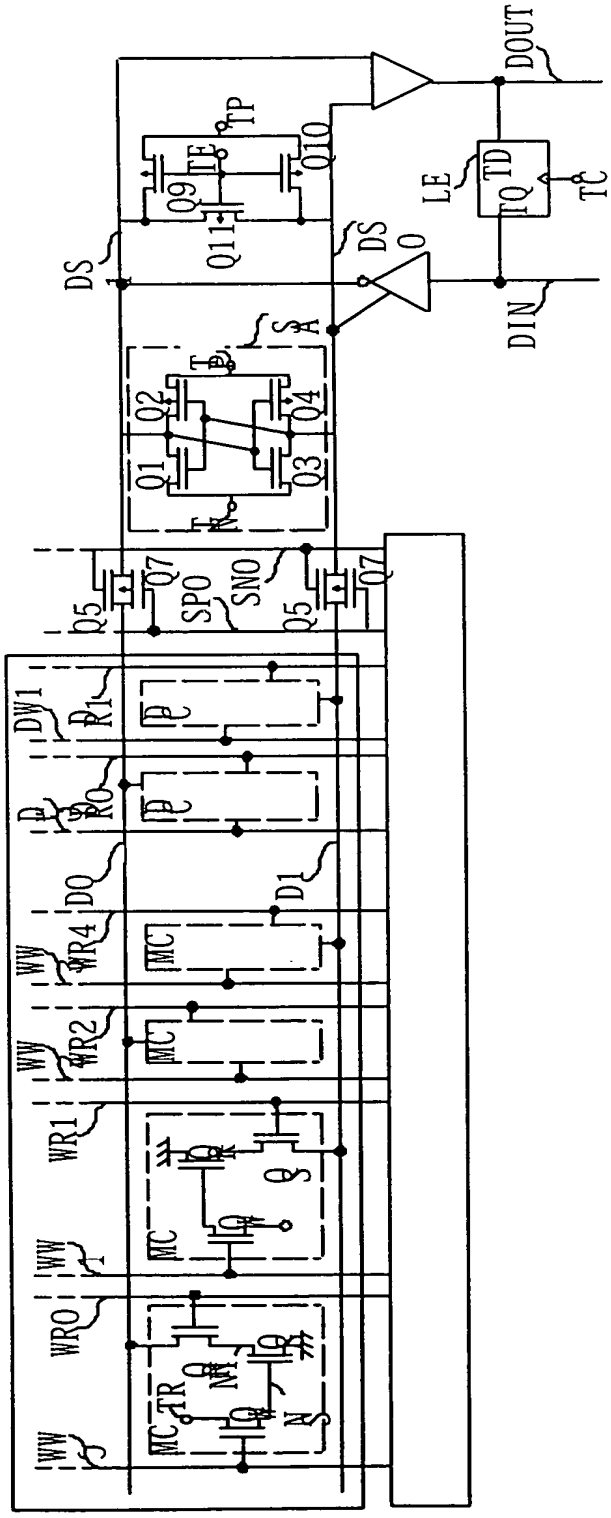

DOUT
DIN
LE
TQ
TD
TC
TP
TE
Q9
Q10
Q11
DS
Q1
Q2
Q3
Q4
Q5
Q7
SPO
SNO
DW1
DW0
DO
D1
WW
WR4
WR2
WR1
WR0
MC
TR

FIG 13

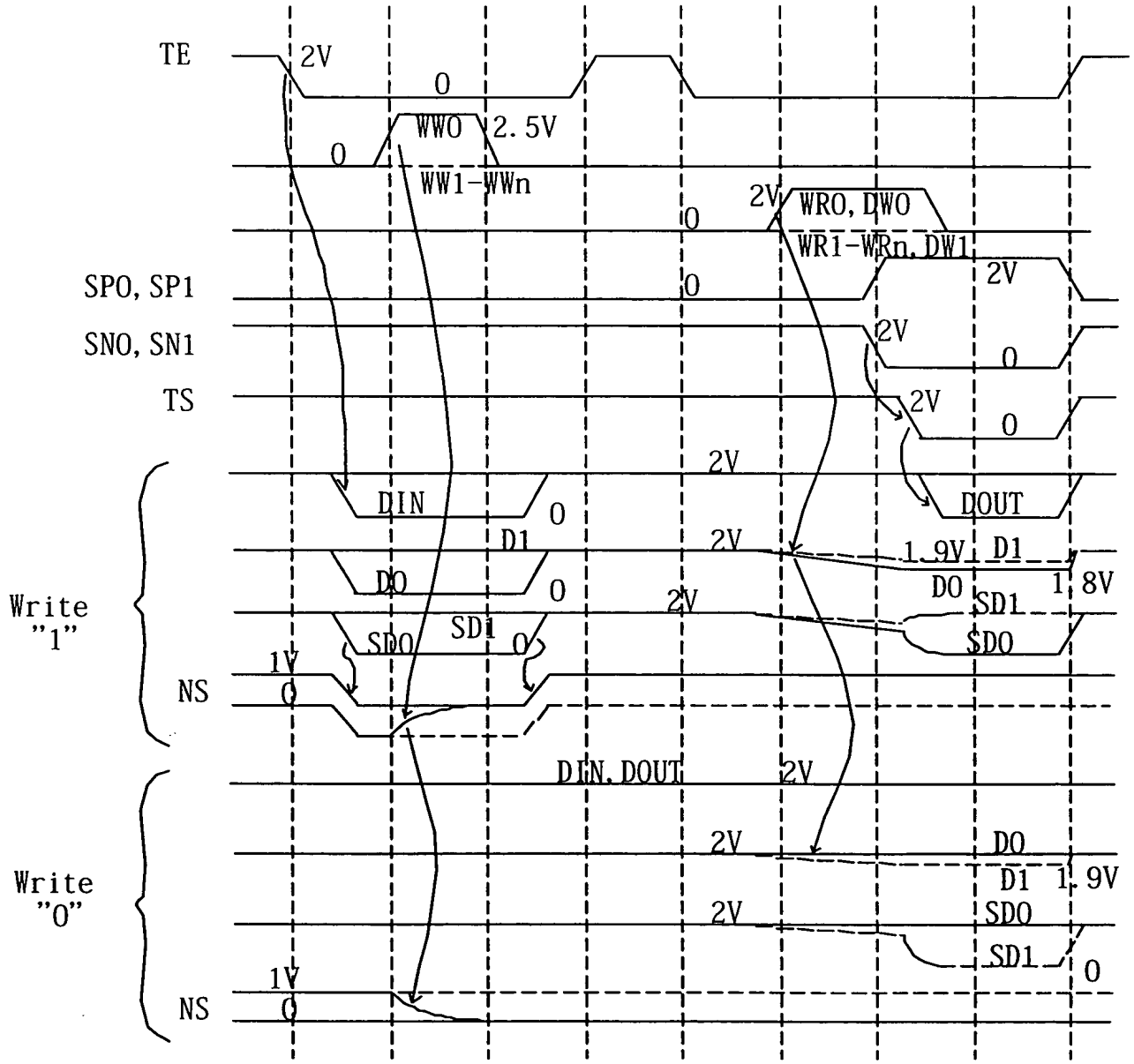

TE
2V
0
WWO
2.5V
WW1-WWn
WRO, DWO
WR1-WRn, DW1
SPO, SP1
SNO, SN1
TS
DIN
DOUT
D1
DO
SD1
SDO
1.9V
1.8V
Write "1"
NS
1V
DIN, DOUT
Write "0"

FIG 14

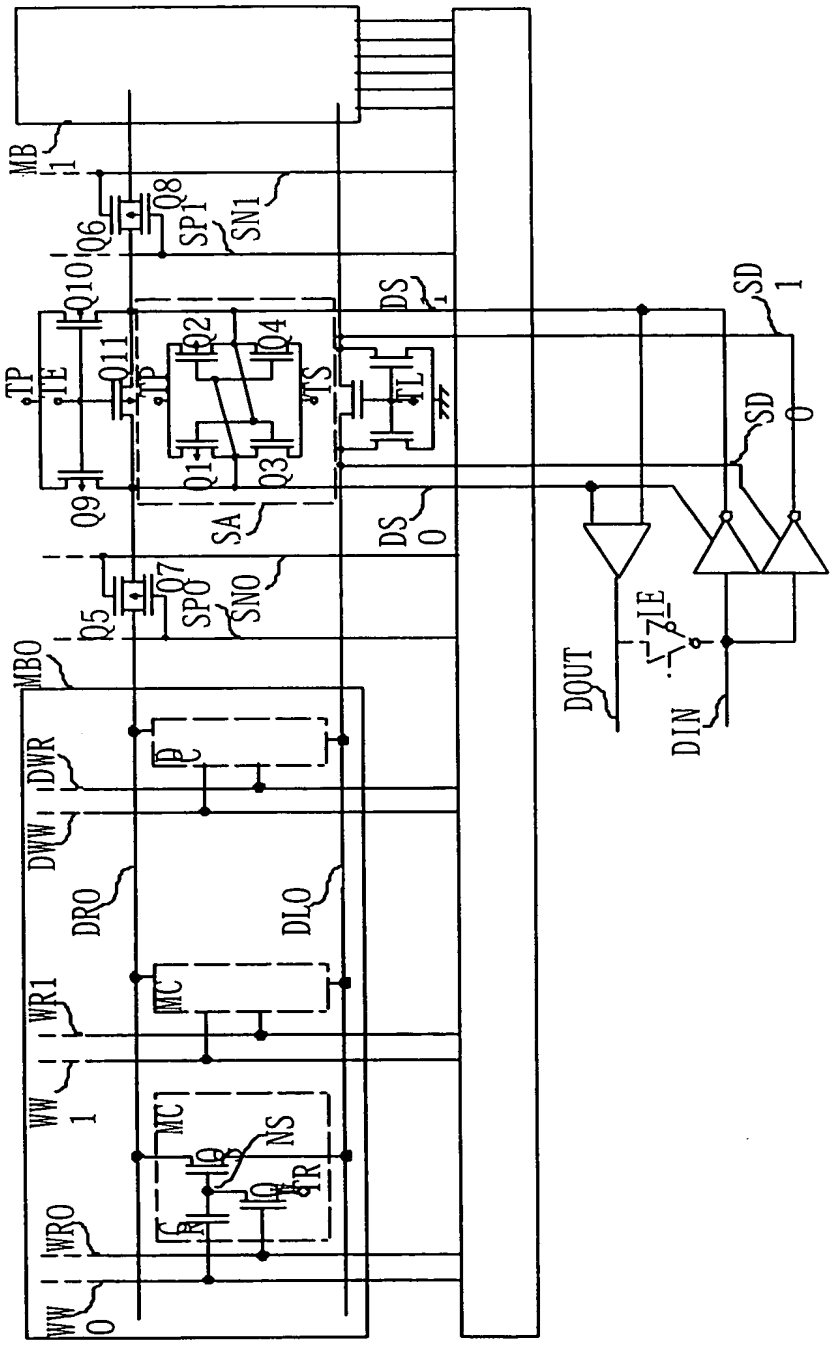

MB 1
Q6
Q8
SP1
SN1
Q10
Q11
TP
TE
TP
Q2
Q4
TS
TL
Q1
Q3
Q9
SA
DS 1
DS 0
SD 1
SD 0
Q5
Q7
SP0
SN0
MB0
DWR
DWW
DR0
DL0
WR1
WW 1
WR0
WW 0
MC
MC1
NS
DOUT
DIN
IE

FIG 15

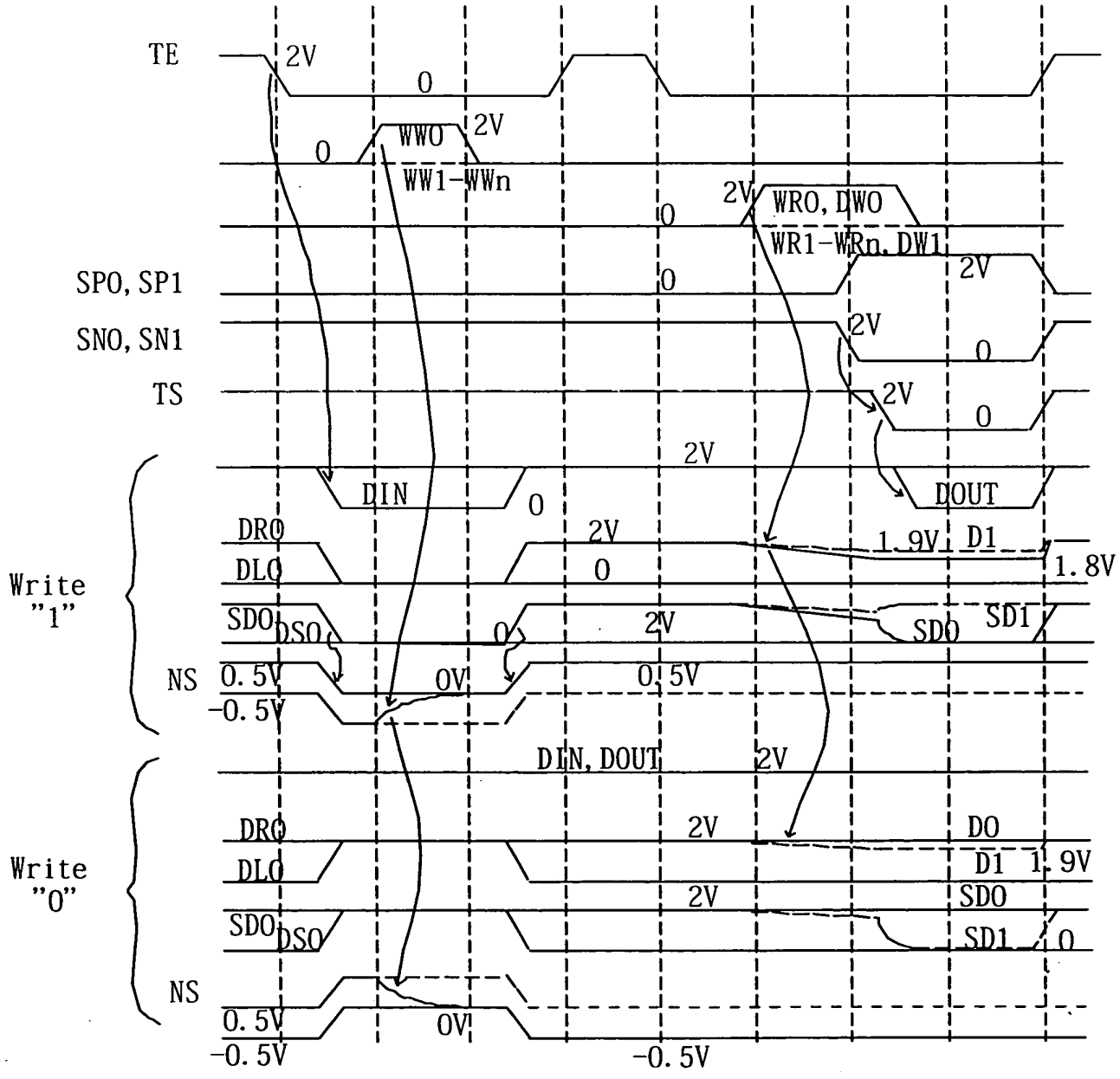

TE
2V
0
WWO
2V
0
WW1-WWn
2V
WRO, DWO
0
WR1-WRn, DW1
2V
SPO, SP1
0
SNO, SN1
2V
0
TS
2V
0
2V
DIN
0
DOUT
DRO
2V
1.9V
D1
1.8V
DLO
0
Write "1"
SDO
DSO
0
2V
SDO
SD1
NS
0.5V
0V
0.5V
-0.5V
DIN, DOUT
2V
DRO
2V
DO
D1
1.9V
DLO
2V
SDO
Write "0"
SDO
DSO
SD1
0
NS
0.5V
0V
-0.5V
-0.5V

FIG 16

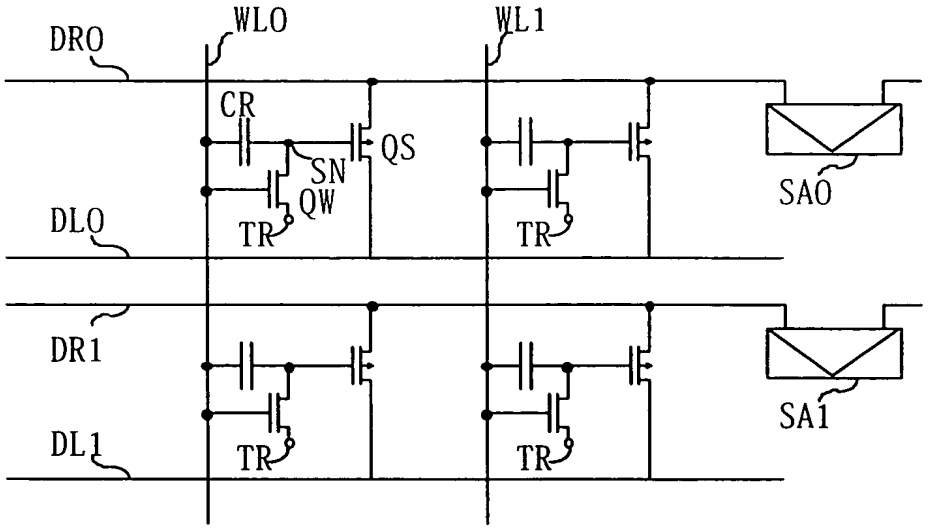


FIG 17A

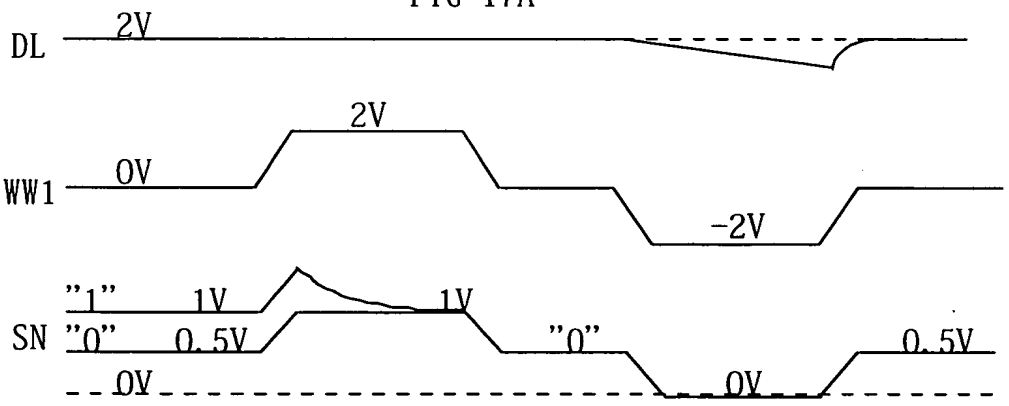


FIG 17B

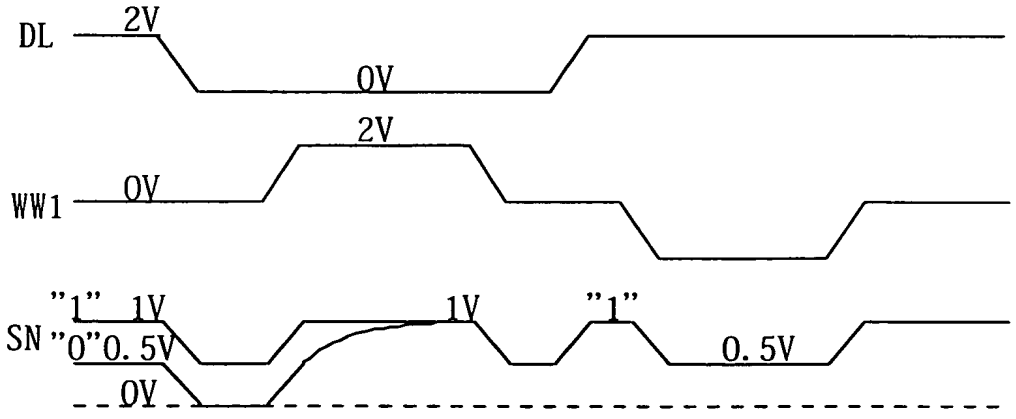


FIG 18

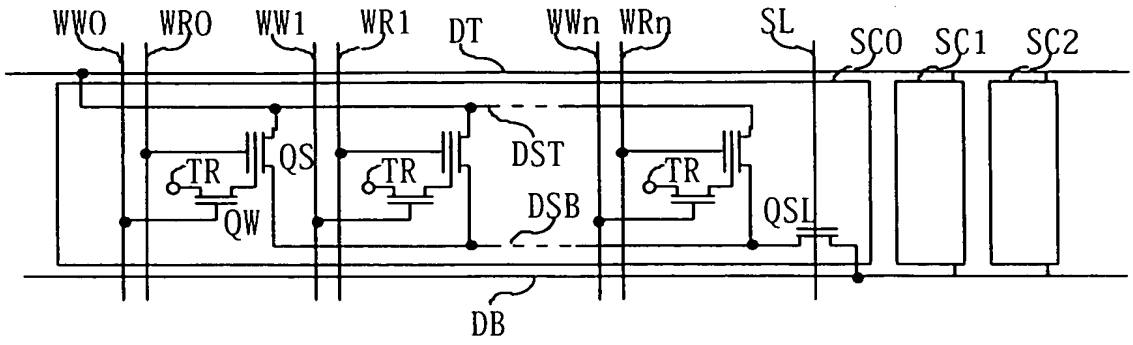


FIG 19A

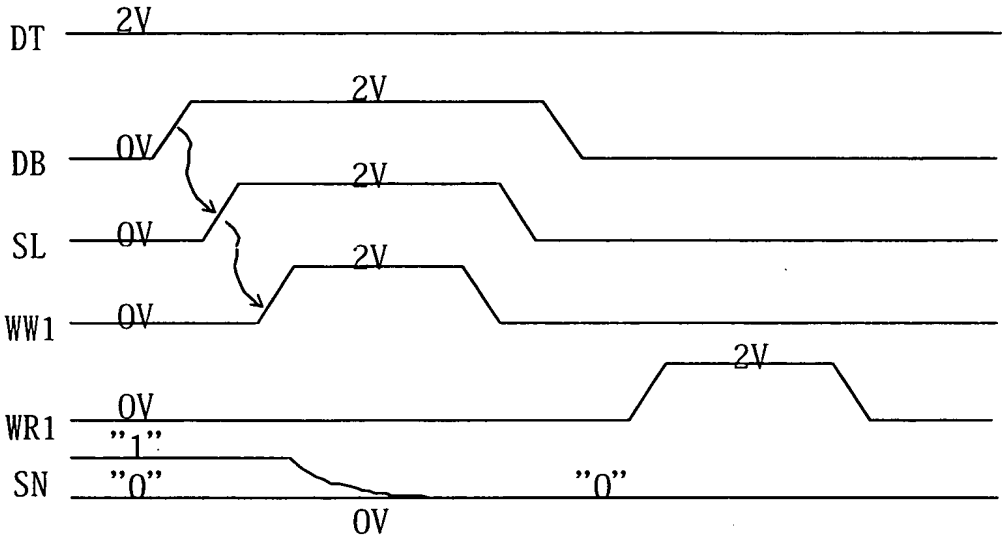


FIG 19B

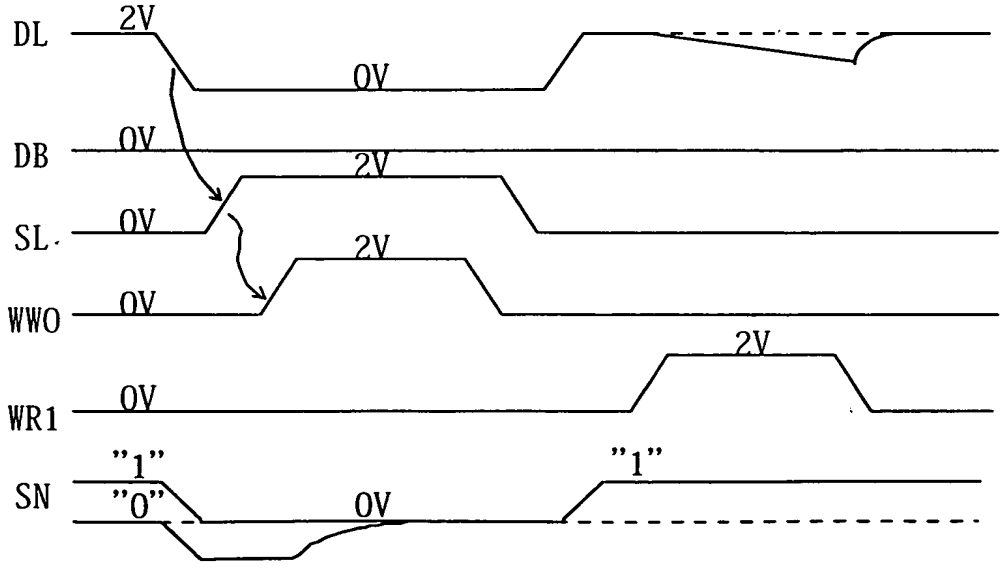


FIG 20

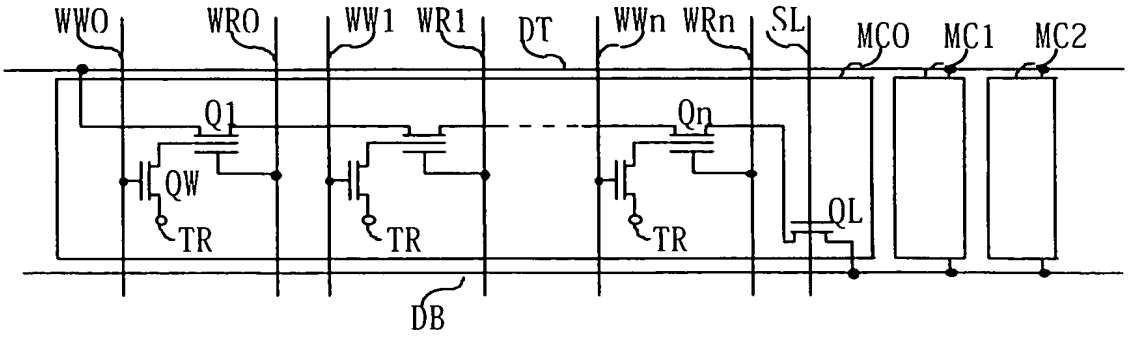


FIG 21A

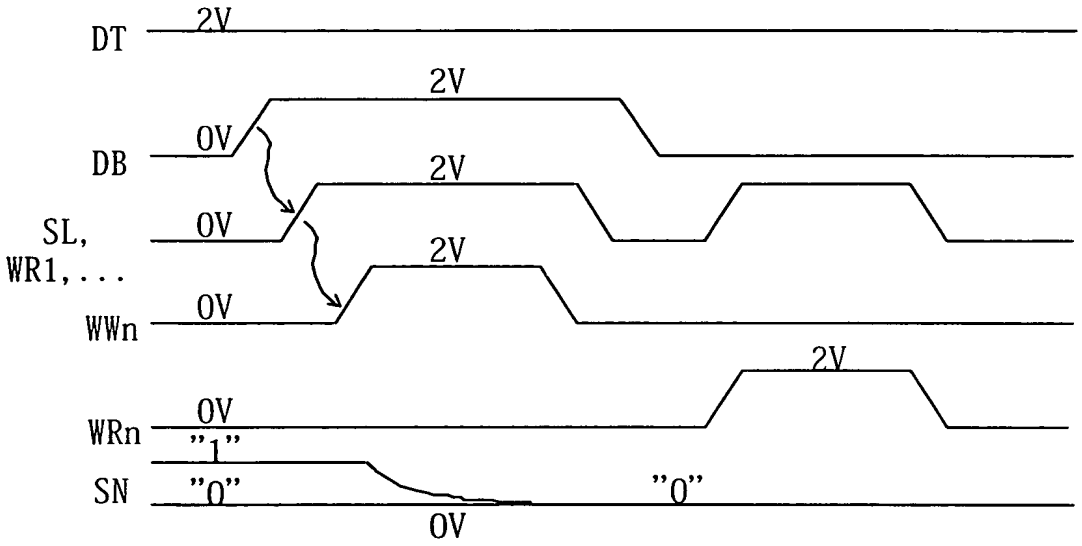


FIG 21B

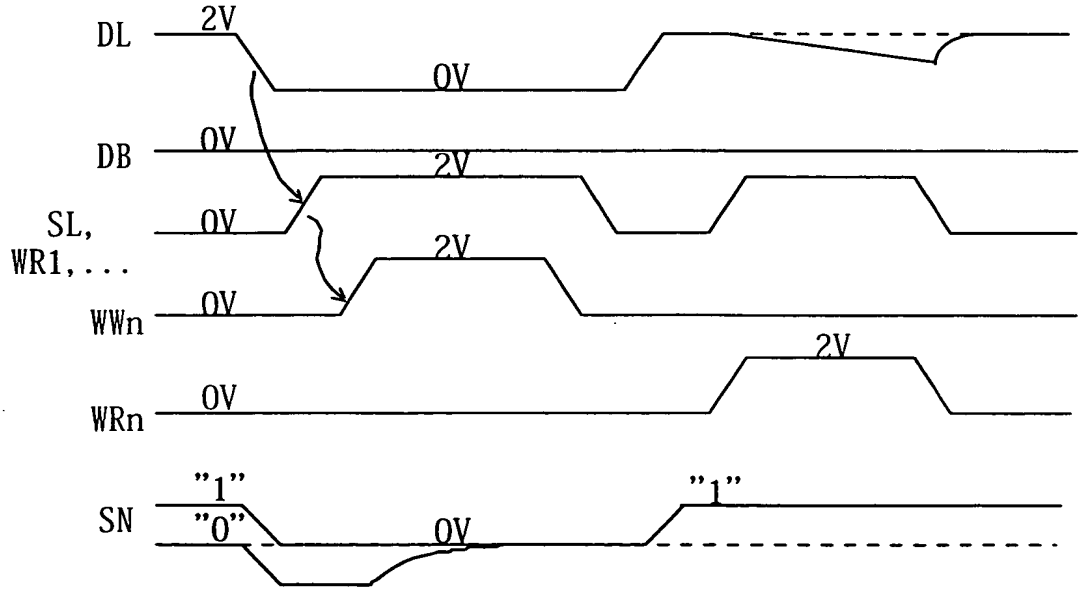


FIG. 22

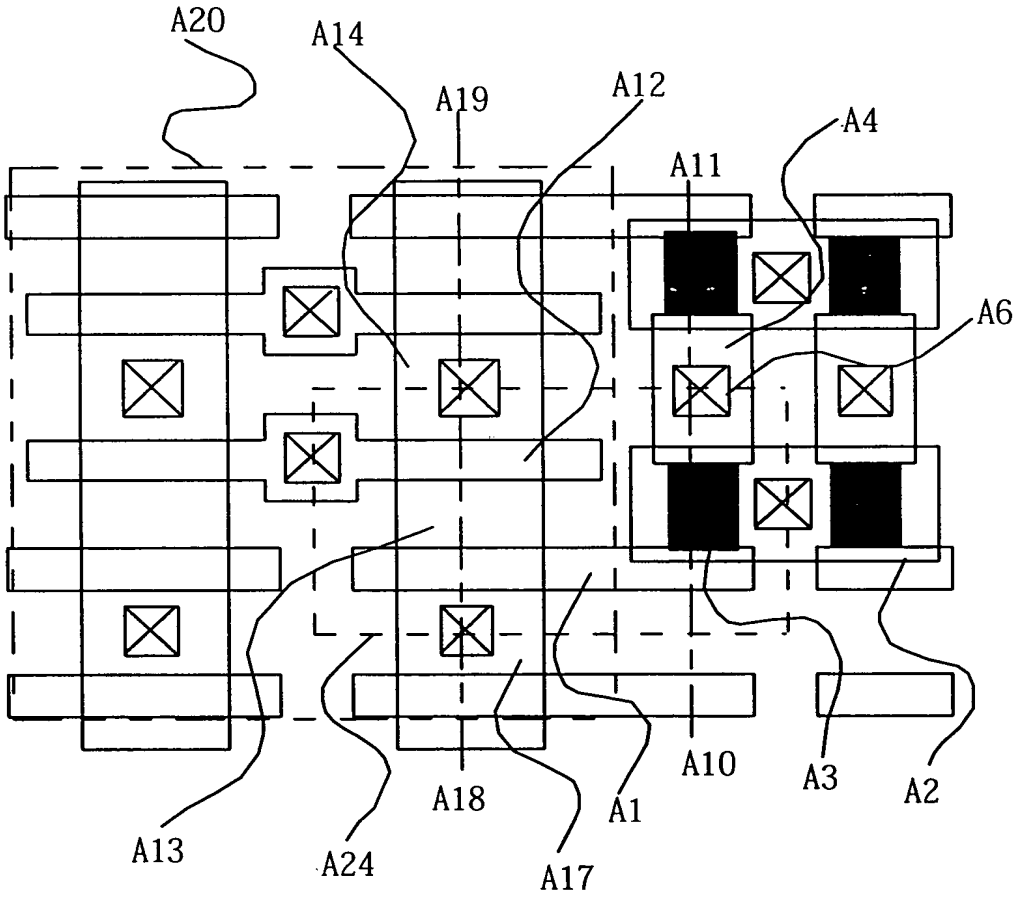


FIG. 23

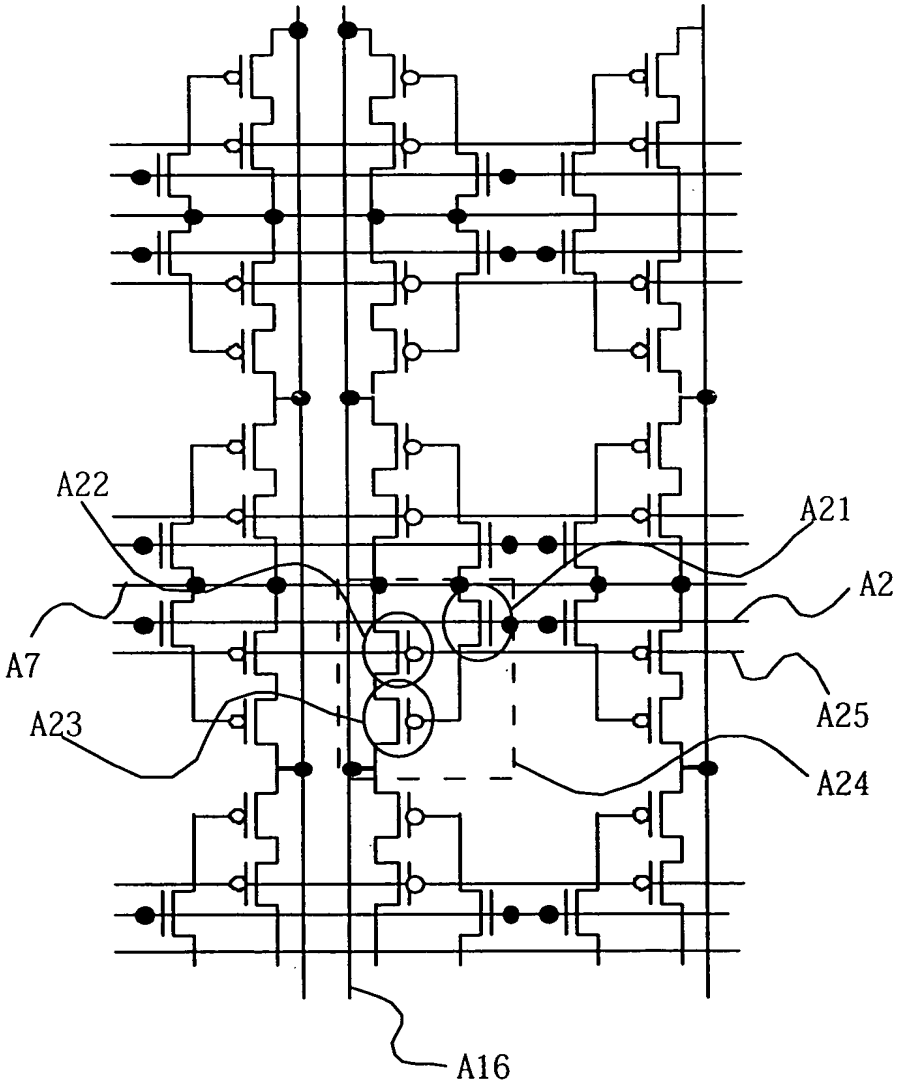


FIG. 24

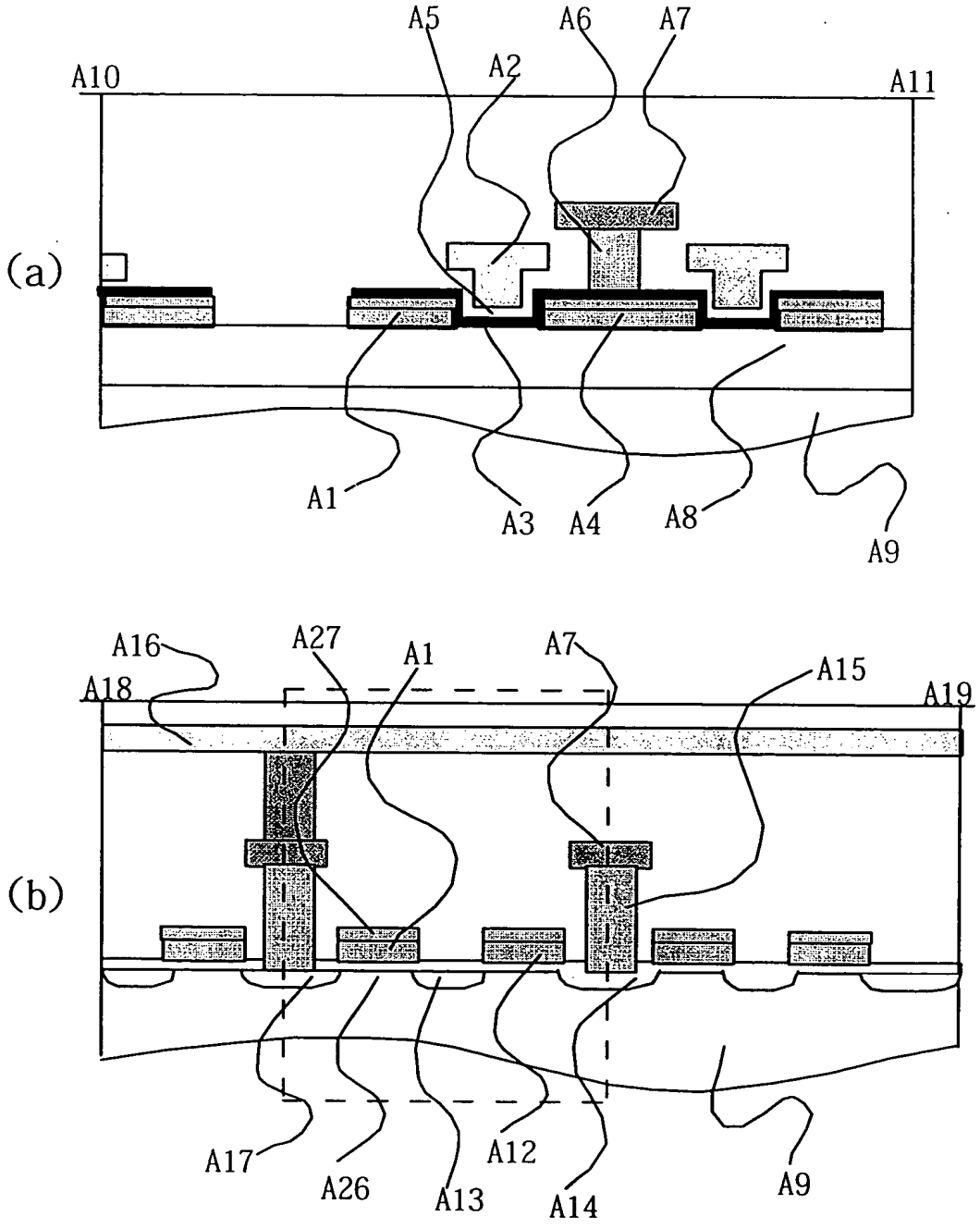

(a)
A5
A6
A7
A2
A10
A11
A1
A3
A4
A8
A9
(b)
A16
A27
A1
A7
A15
A18
A19
A17
A26
A13
A12
A14
A9

FIG. 25

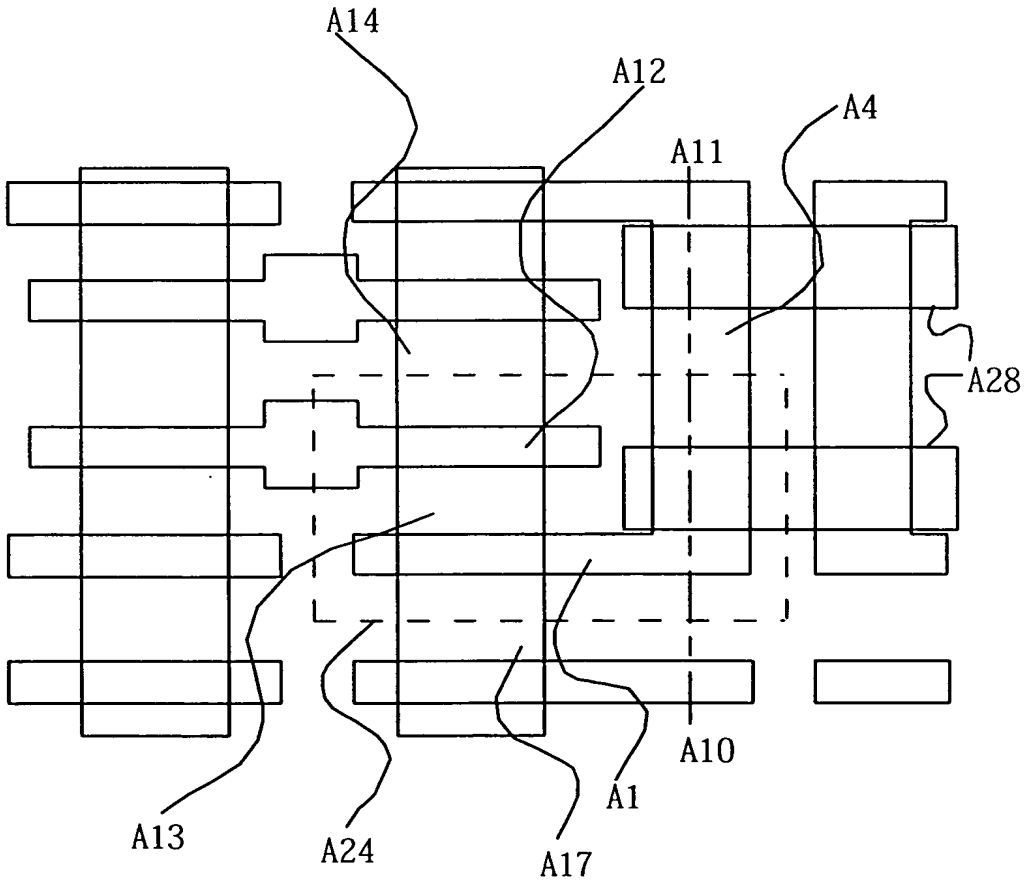


FIG. 26

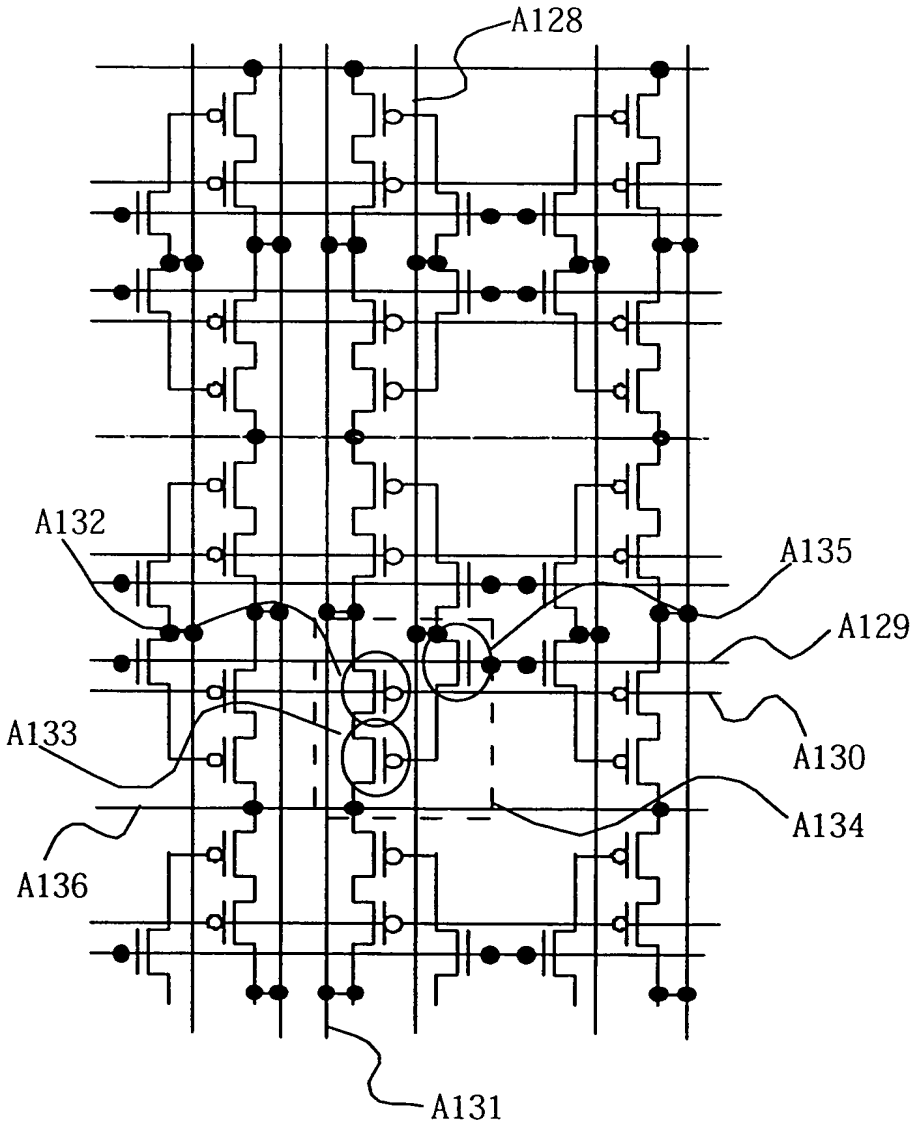


FIG. 27

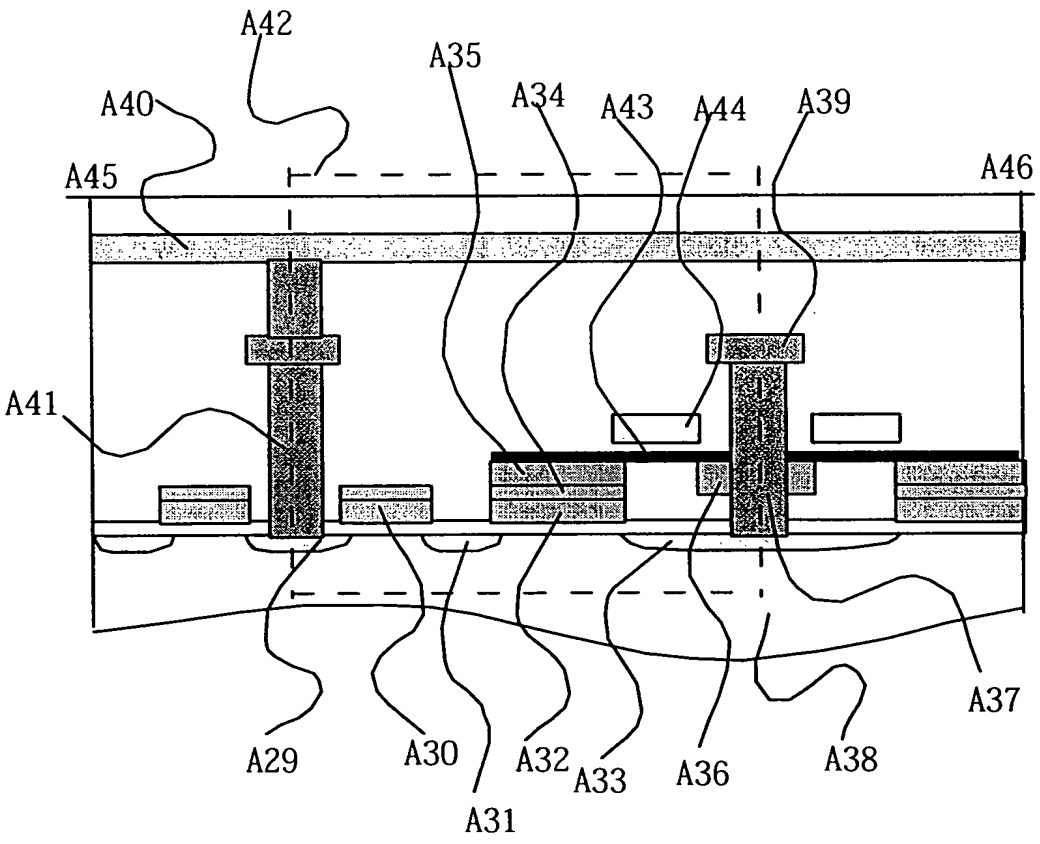

A42
A35
A40
A34
A43
A44
A39
A45
A46
A41
A37
A29
A30
A32
A33
A36
A38
A31

FIG. 28

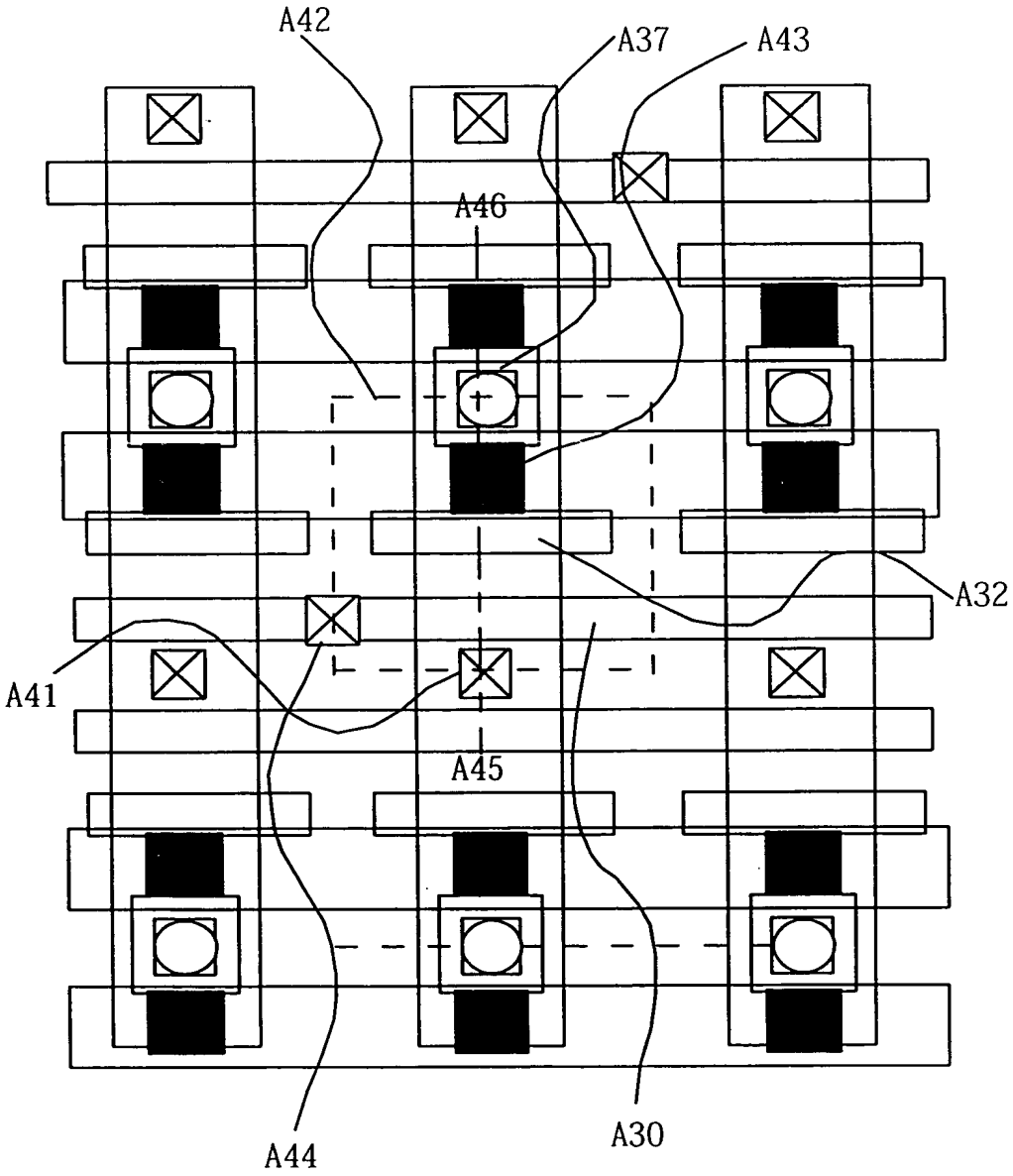


FIG. 29

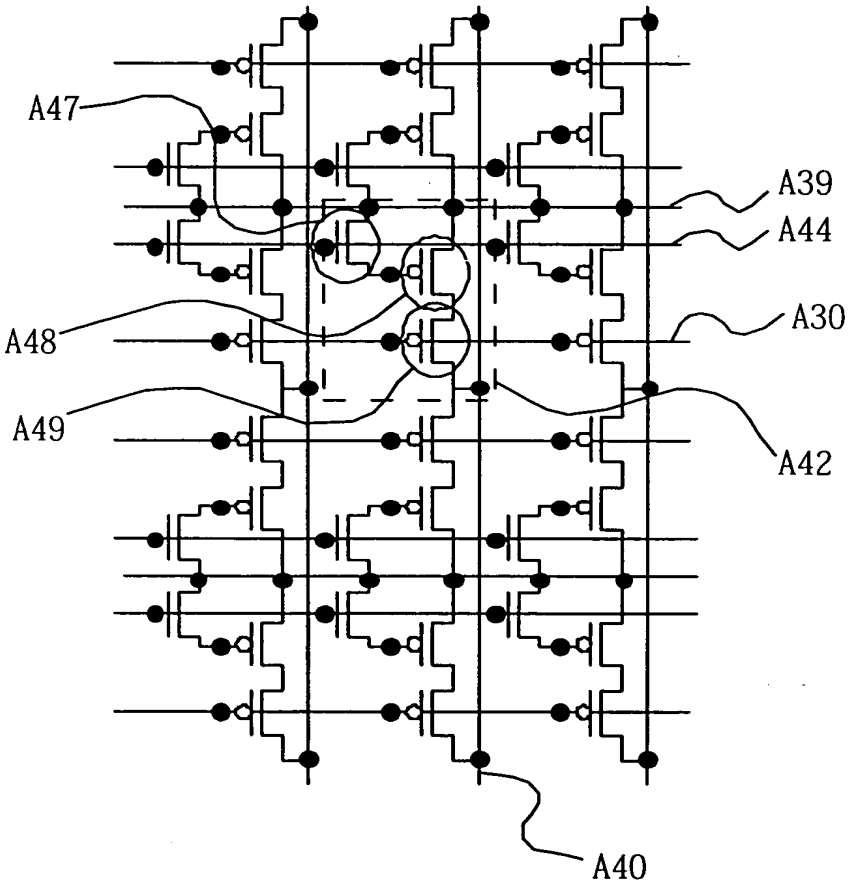


FIG. 30

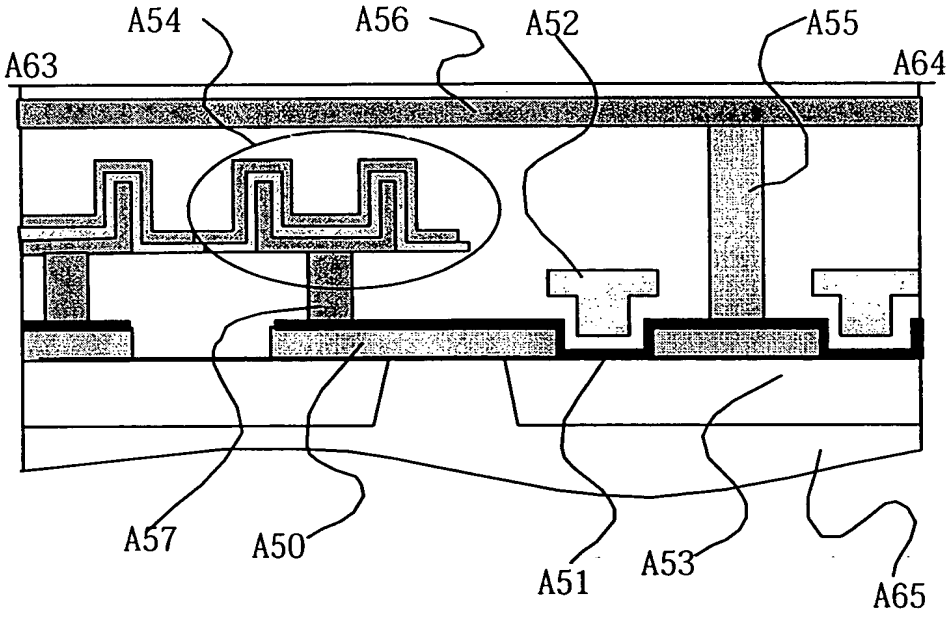


FIG. 31

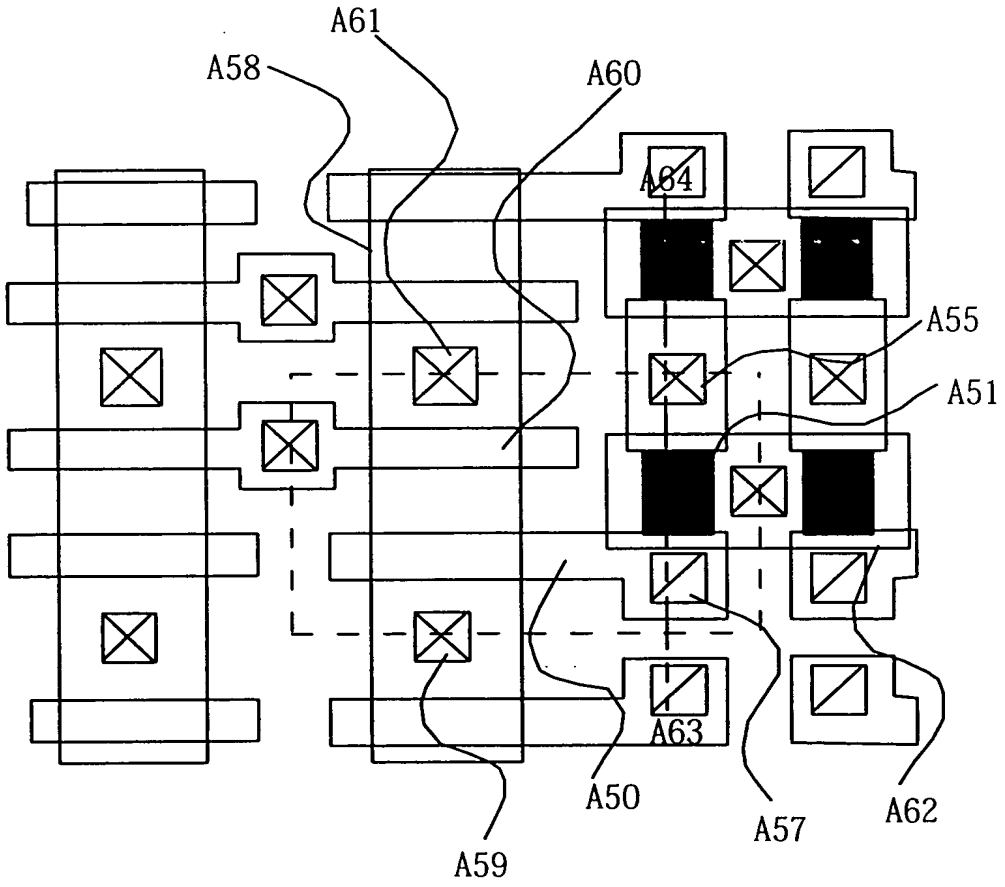


FIG. 32

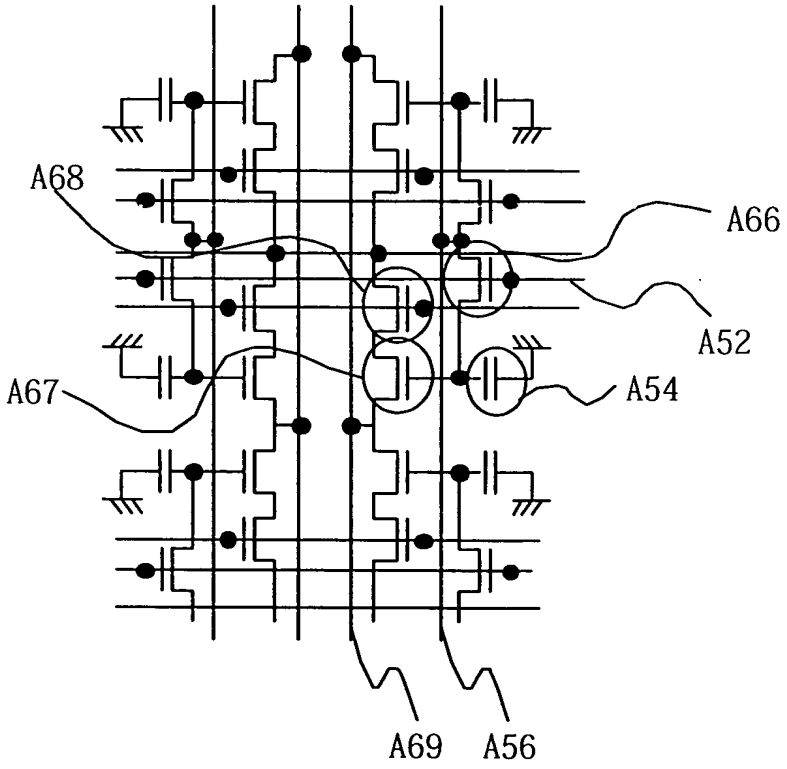


FIG. 33

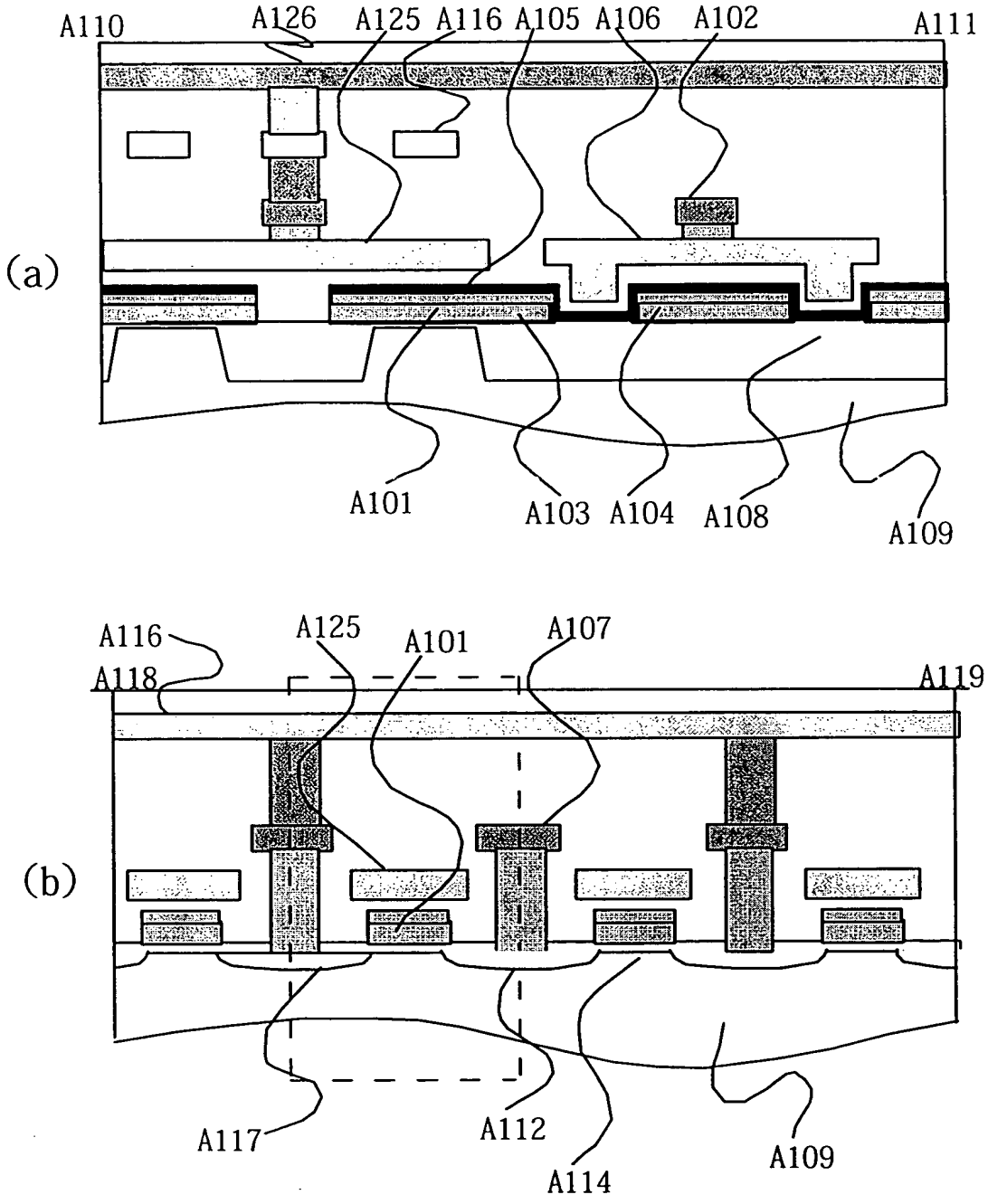

(a)
A110
A126
A125
A116
A105
A106
A102
A111
A101
A103
A104
A108
A109
(b)
A116
A118
A125
A101
A107
A119
A117
A112
A114
A109

FIG. 34

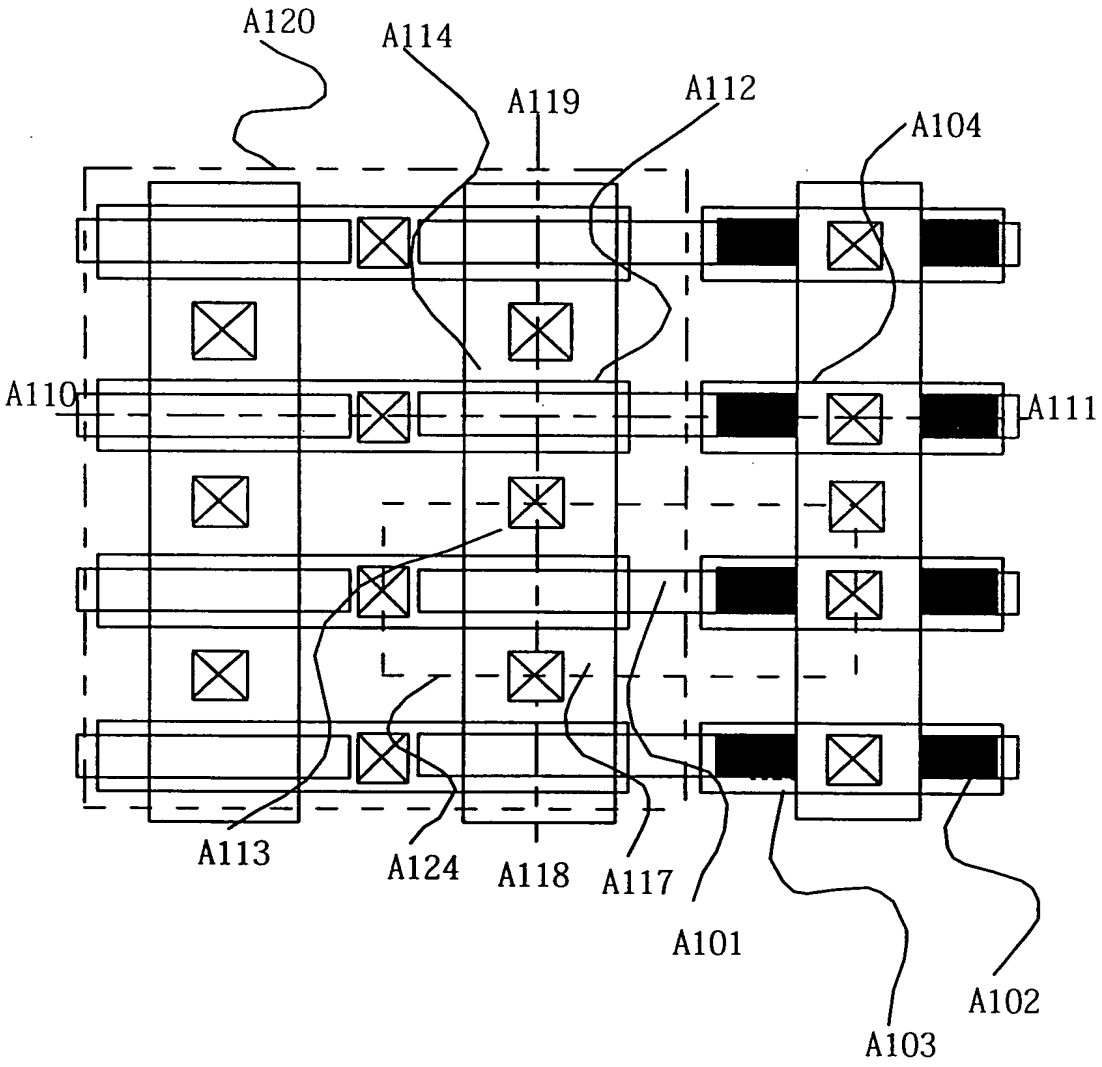

A120
A114
A119
A112
A104
A110
A111
A113
A124
A118
A117
A101
A102
A103

FIG. 35

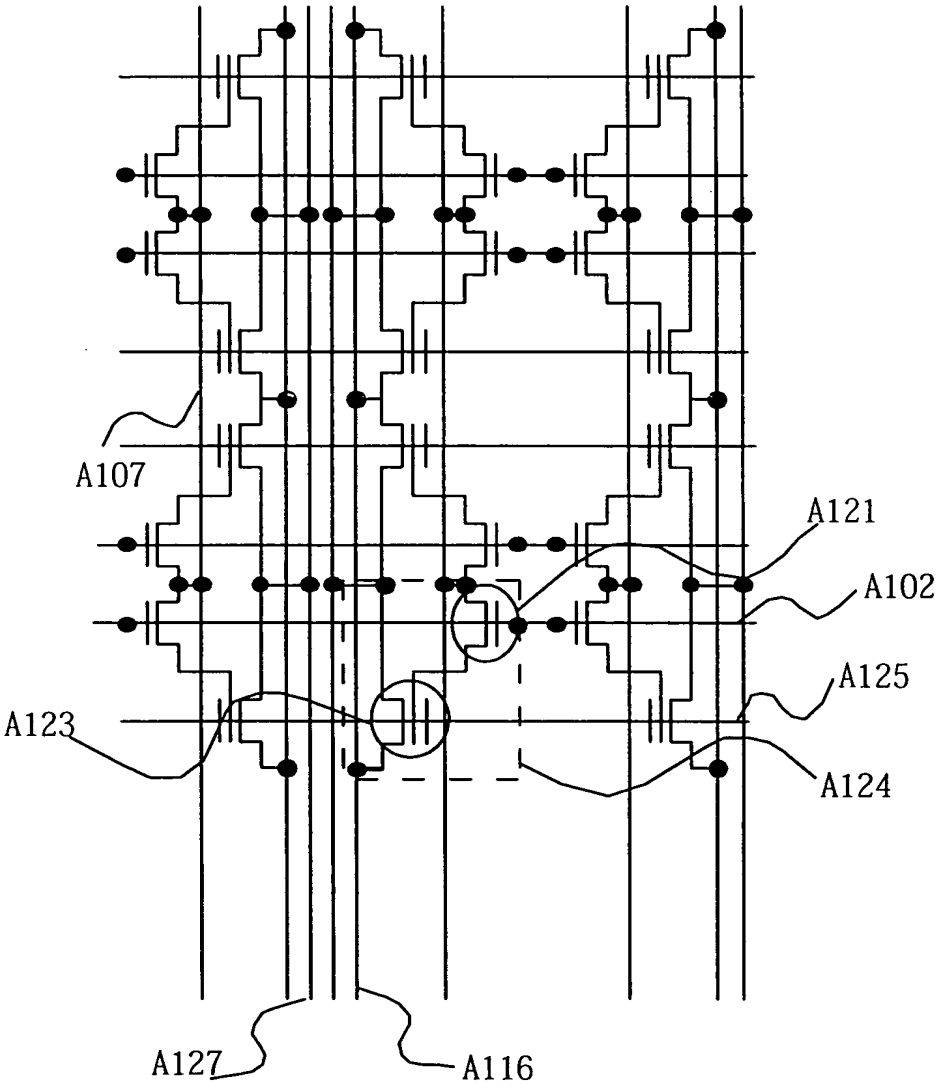


FIG. 36

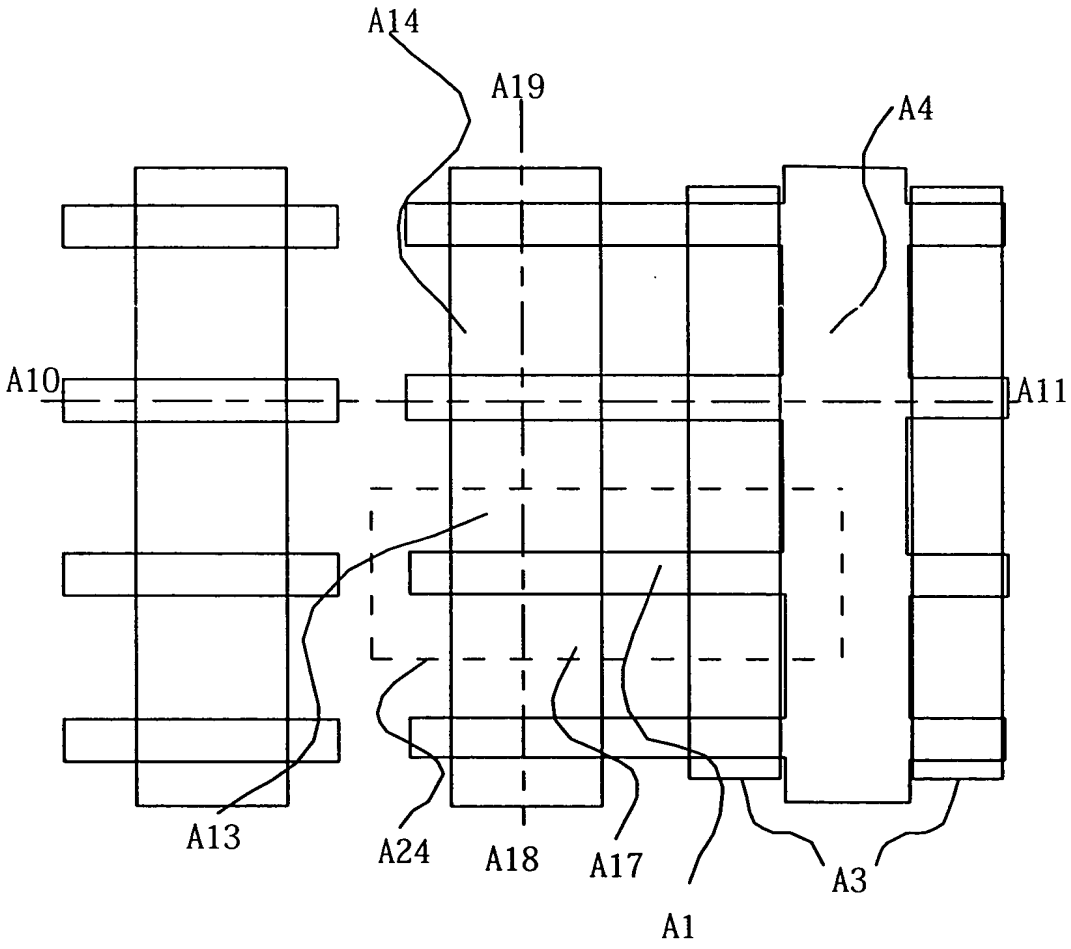


FIG 37

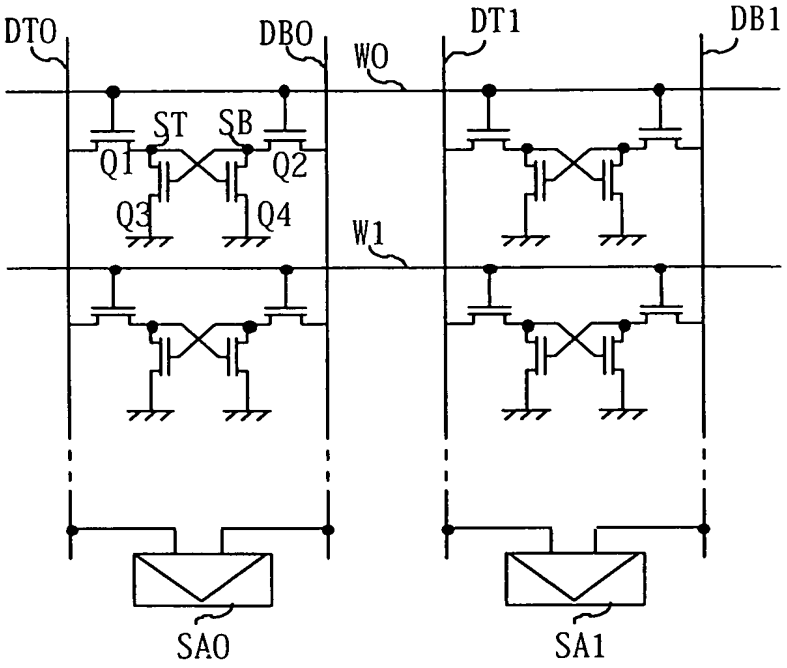


FIG 38A

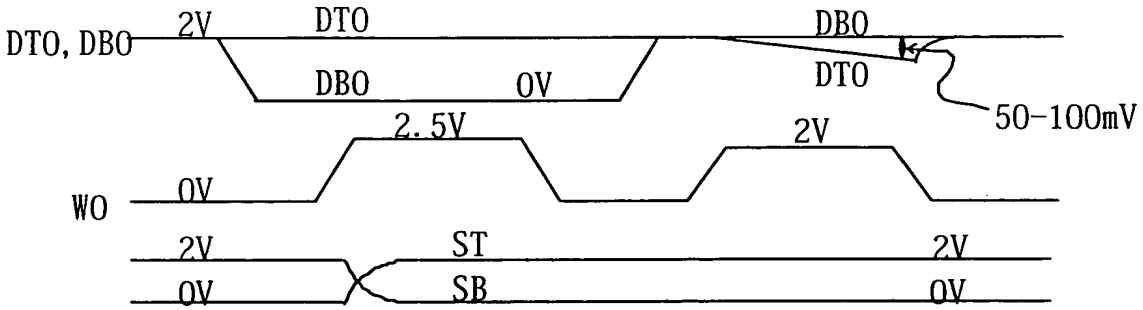


FIG 38B

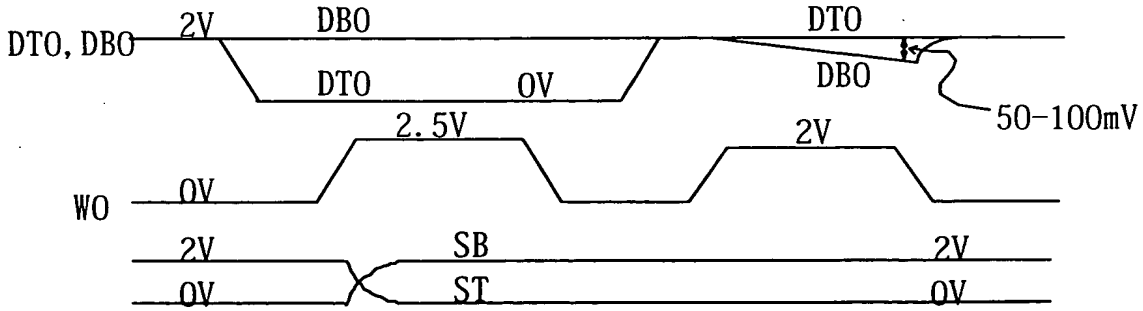


FIG 39

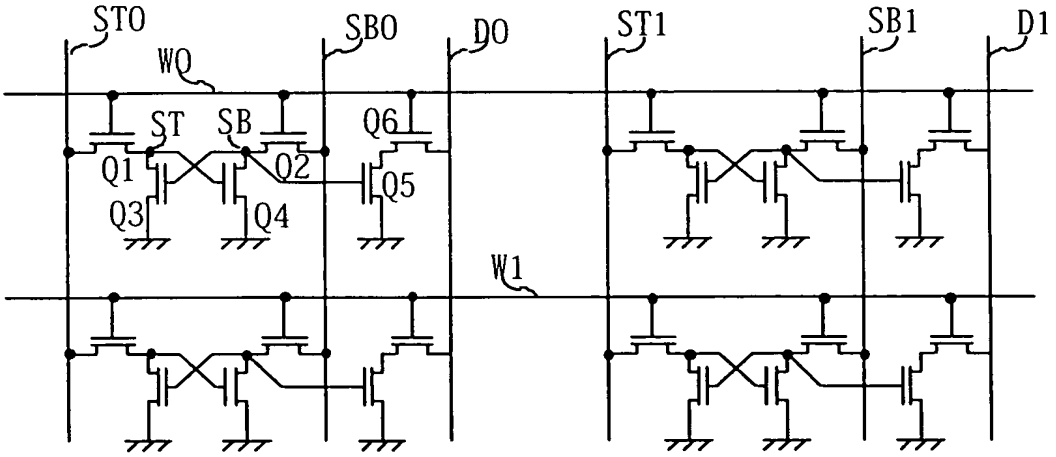


FIG 40A

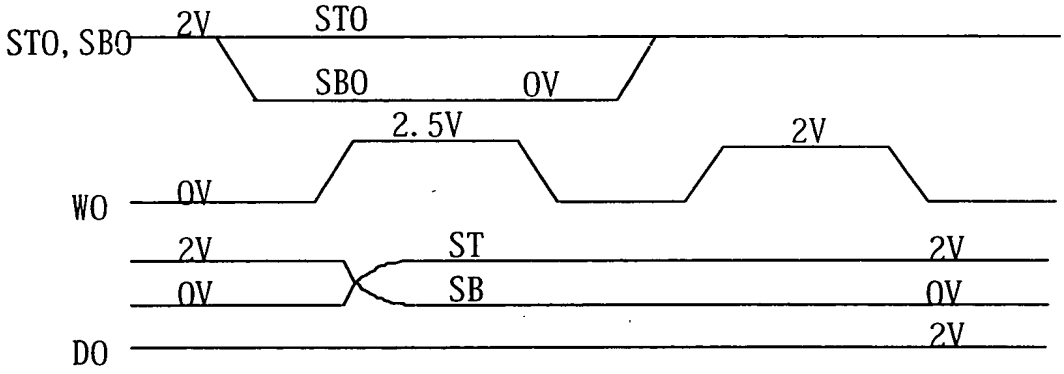


FIG 40B

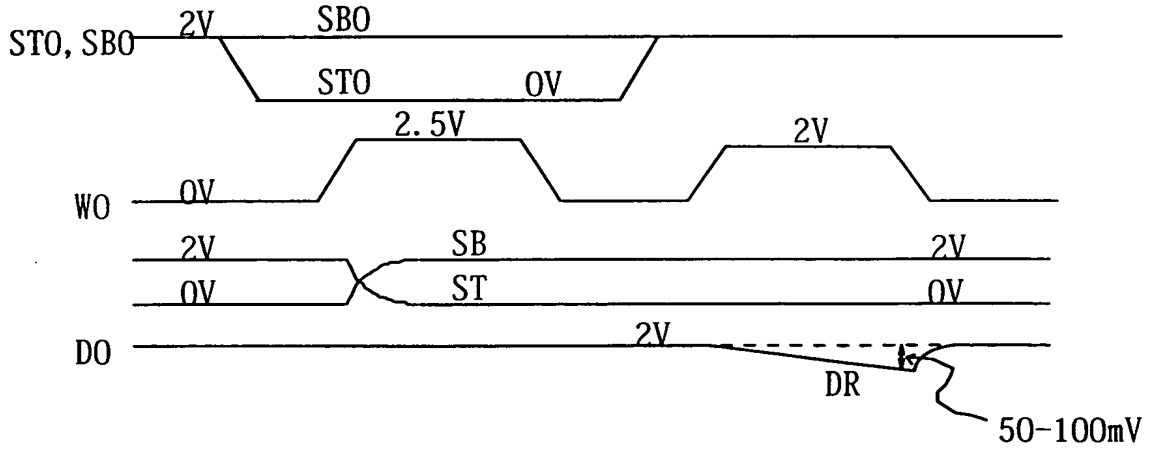


FIG. 41

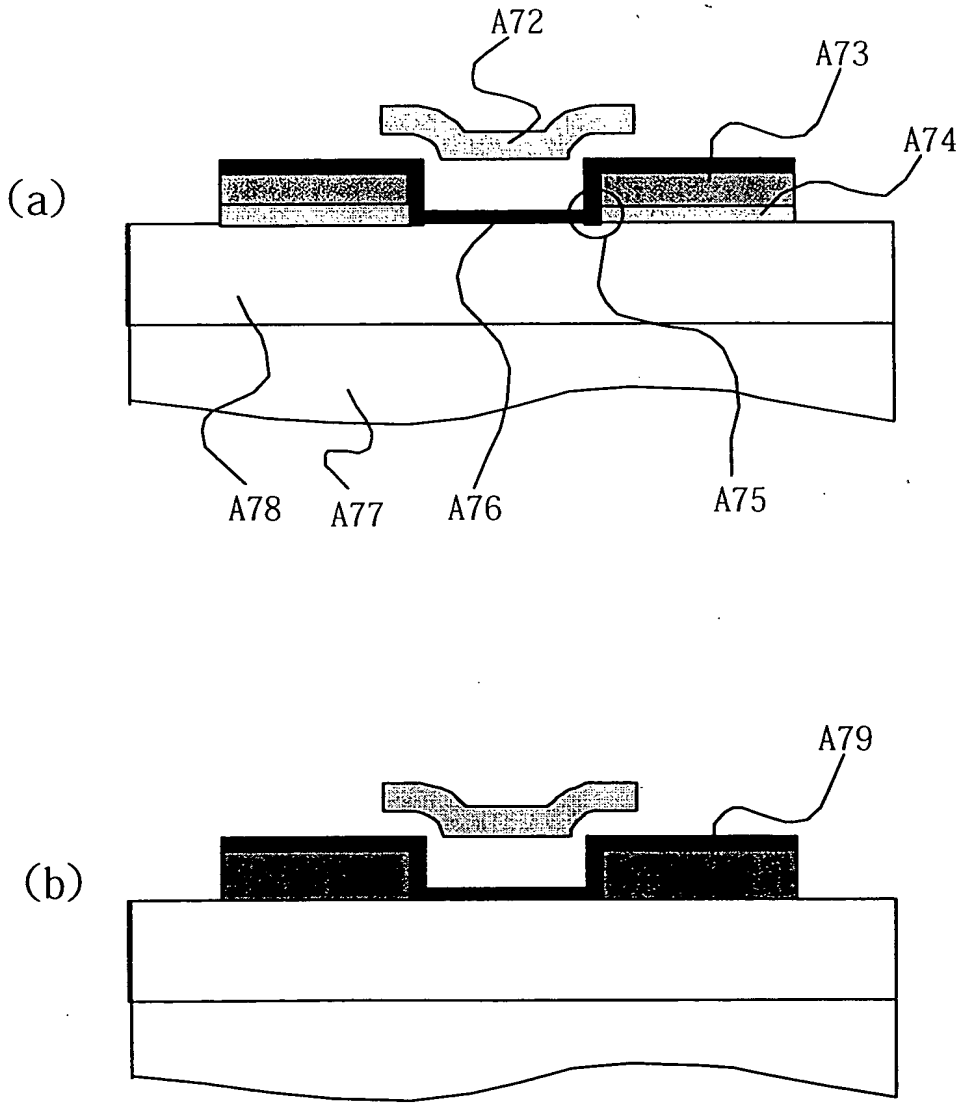


FIG. 42

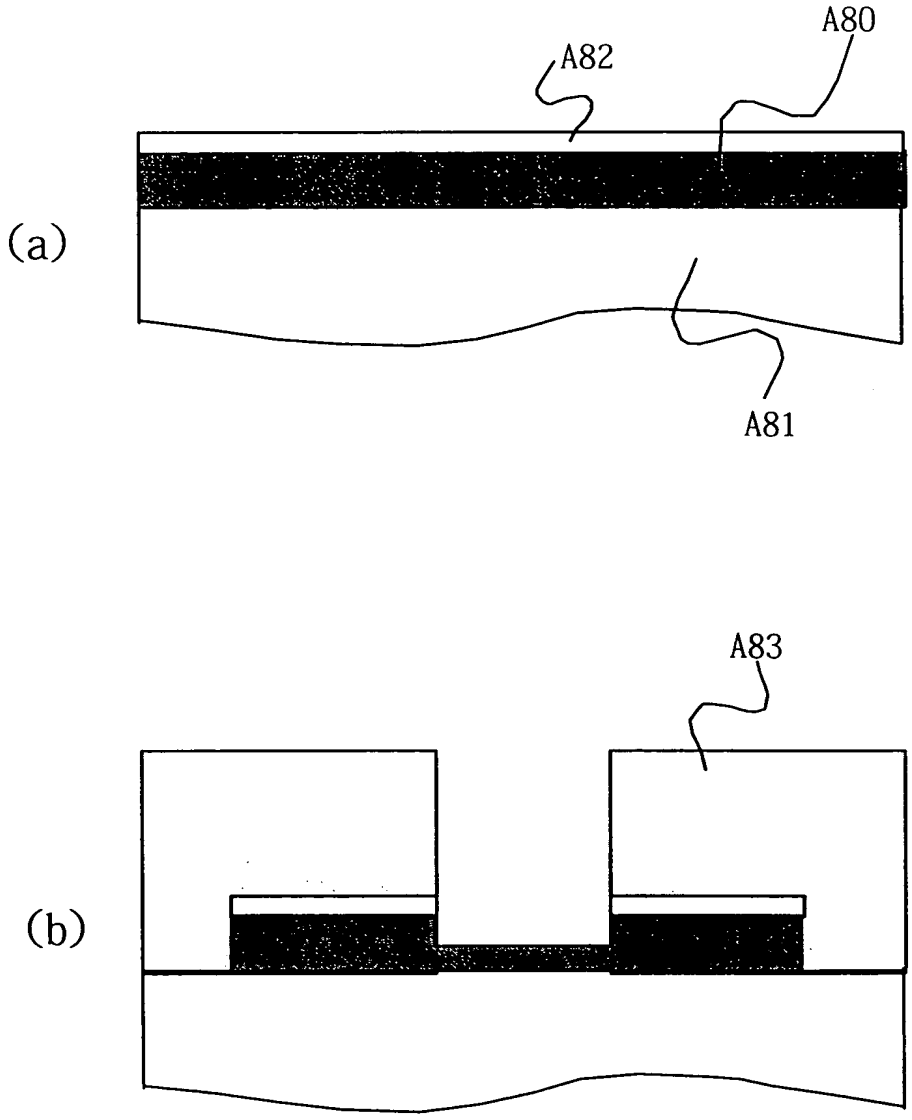


FIG. 43

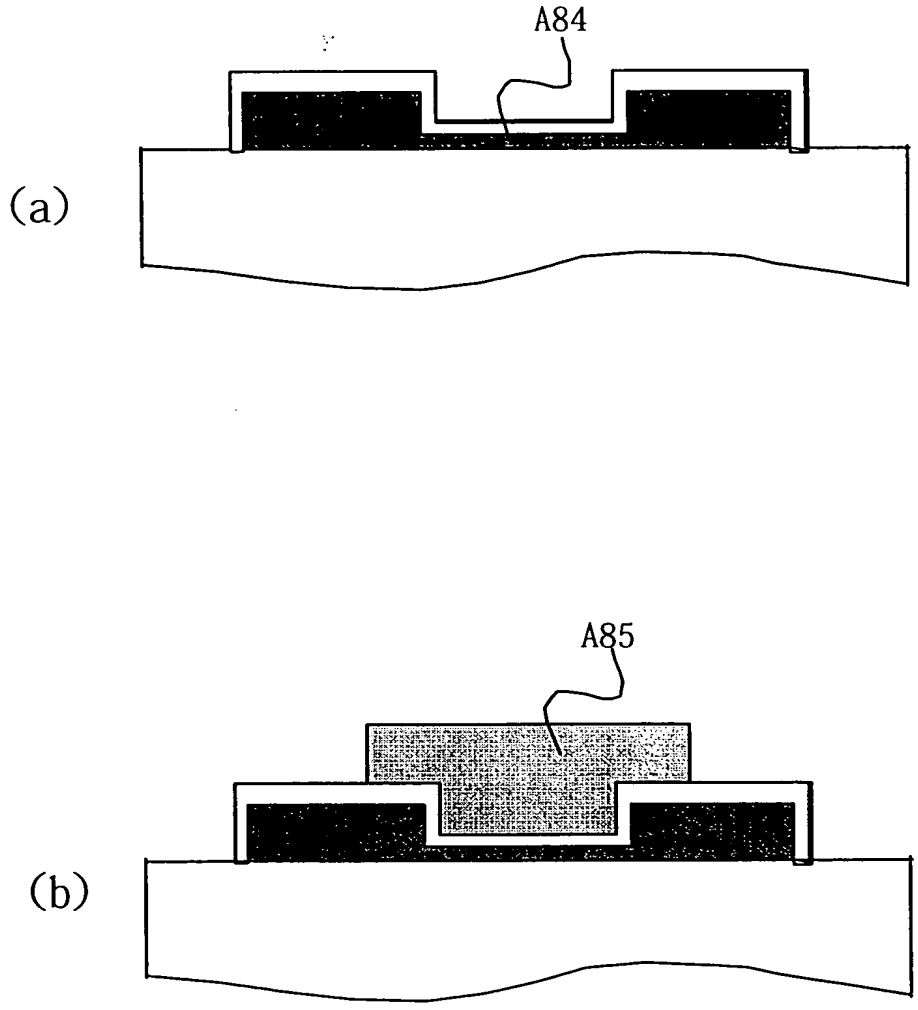


FIG. 44